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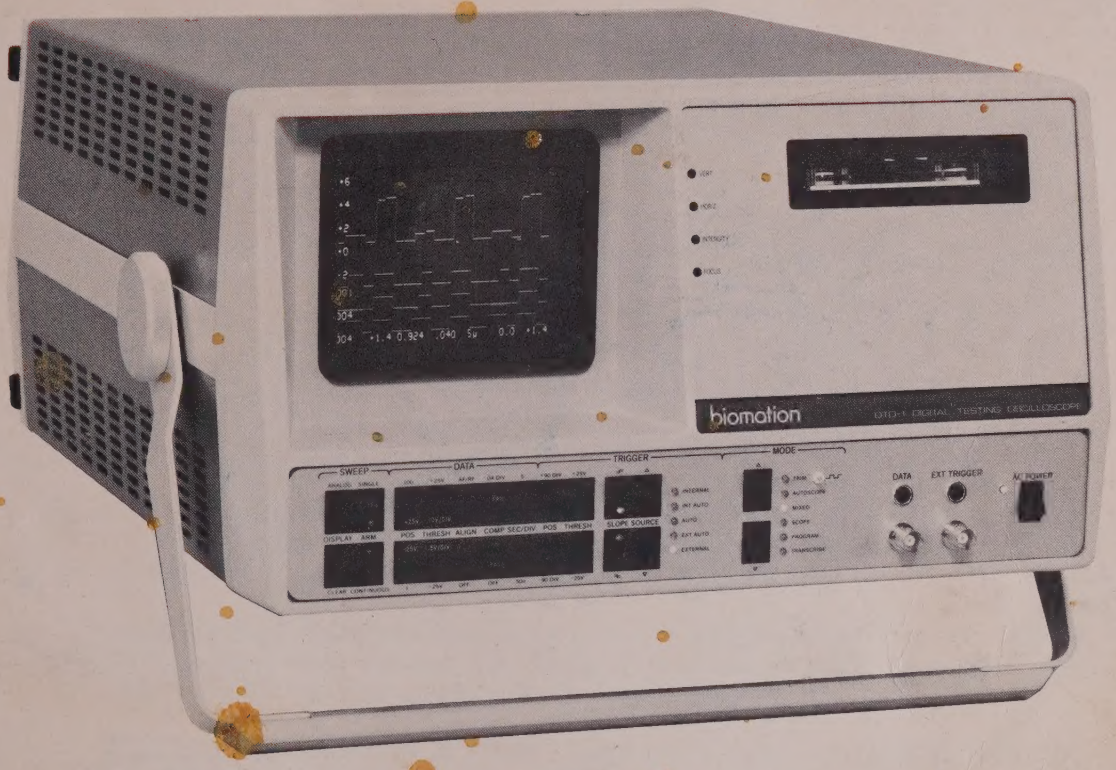

MODEL DTO-1
DIGITAL TESTING OSCILLOSCOPE

OPERATING AND SERVICE MANUAL

PRELIMINARY

MP MASTER
MA34671

Gould Inc., Biomation Division 4600 Old Ironsides Drive, Santa Clara, CA 95050
(408) 988-6800 TWX: 910-338-0509 Printed in U.S.A.

GOULD

IMPORTANT NOTE

This preliminary manual is supplied to permit earliest possible delivery of instruments. Additional and more complete information will be included in a subsequent final edition of this manual.

Under normal circumstances, all owners of Model DTO-1 Digital Testing Oscilloscopes who receive this preliminary manual with their unit will automatically receive a copy of the final edition.

IF FOR SOME REASON A FINAL EDITION IS NOT RECEIVED, PLEASE CONTACT THE GOULD INC., BIOMATION DIVISION FACTORY, GIVE THE SERIAL NUMBER OF THE UNIT AND COMPLETE RETURN ADDRESS INFORMATION.

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DTO-1 PRELIMINARY MANUAL UPDATES

FIRMWARE CHANGE

ROM has been expanded from 14K to 16K bytes to accommodate the following operational changes.

OPERATION CHANGES

1. TRIGGER POS, +90 DIV and -90 DIV is changed to +180 DIV and -180 DIV in Figure 3.1.

2. Trigger position is settable to $\pm$ 180 divisions in the SCOPE mode and to $\pm$130 divisions in the PROGRAM mode.

3. In the ALIGN mode, the "R" traces are adjusted with reference to the center of the display instead of the trigger point. This eliminates the possibility of the "R" traces being shifted off screen. The trigger position is adjusted to the align ratio and displayed. All displayed waveforms remain on a common time scale.

4. A "REWIND TAPE" function has been added in the TRANSCRIBE mode. The tape will also automatically rewind, prior to indexing the tape, in either the ERASE or PROGRAM modes. It is recommended that a new data cartridge be rewound before using. The following is the "Operation Environment" for the DC100A data cartridge:

Operation Environment	
Temperature	32 to 122°F (0 to 50°C)
RH	20 to 80% non-condensing
Maximum Wet Bulb Temperature	79°F (26°C)

3M recommends that if the recipient of a data cartridge knows or suspects that the cartridge has been exposed to either the maximum or minimum temperature extreme, that it be rewound one complete cycle before using.

OPERATING AND SERVICE MANUAL

MODEL DTO-1

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SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument was thoroughly tested and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'S WARRANTY, GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Instrument Description

The Model DTO-1 Digital Testing Oscilloscope is a multipurpose instrument used for the design, test, and maintenance of digital equipment. Among its many features is the ability to compare automatically logic traces from a unit under test against prerecorded logic traces from a known good system.

The DTO-1 is basically a logic recorder that digitizes signals one at a time and displays up to eight logic traces on a common time scale. These logic traces can provide pretrigger and/or delayed information. Digitized signals and their associated attributes can also be stored on magnetic tape, then recalled for logic trace display at a later date. Logic traces from magnetic tape and logic traces from newly digitized signals can appear simultaneously on a common time scale. The "old" traces can be automatically expanded or compressed up to 25% to compensate for differences in clock rates between the "old" traces and the "new" traces. Each "new" trace can be automatically compared to a corresponding trace from magnetic tape to determine whether disagreements are within acceptable limits. The result of this comparison is indicated by PASS/FAIL LEDs. The exact areas of logical disagreement are also underscored on the display.

In addition, a signal can be digitized to one part in 39. The resulting analog waveform and up to three logic traces can be simultaneously displayed on a common time scale.

1.4 Specifications

INPUTS

Data (Referred to tip of probe).

Impedance. 10 MΩ, 15 pF.

Voltage range. ±25 V, protected to ±200 V.

Threshold voltage. ±25 V, adjustable in 0.1 V steps, accurate to ±100 MV ±3% of reading.

Minimum pulse width. 10 ns when 50% or more of pulse height exceeds the threshold voltage.

Sample rate. 2 Hz to 100 MHz, accurate to 0.1%.

Number of bits stored. 1000 per trigger event.

Resolution* of stored bits. 50 ns to 1 µs/div -- 10 ns. 2 µs to 5 s/div -- $\frac{s/div}{100}$.

Trigger (Referred to tip of probe).

Impedance. 10 MΩ, 15 pF.

Voltage range. ±25 V, protected to ±200 V.

Threshold voltage. ±25 V, adjustable in 0.1 V steps, accurate to ±200 mV ±3% of reading.

Minimum pulse width. 20 ns when 50% or more of pulse height exceeds the threshold voltage.

Source. Internal, Internal Auto, Auto, External Auto and External.

Slope. Positive or Negative.

Position (Referred to one division from left side of display). -90 divisions to +90 divisions in 0.1 division steps, accurate to ±0.1% of reading ±2 samples.

COMPARE

Resolution*. 50 ns to 1 µs/div -- 40 ns. 2 µs to 5 s/div -- 4X $\frac{s/div}{100}$.

OUTPUT

Probe Calibration Signal. 1 kHz squarewave 0 to +4 V.

Auxiliary Power for Optional 10-TC Pod. +5 V ±0.25 V, 360 mA; -5.2 V ±0.2 V, 100 mA.

TIME BASE

Sweep Ranges. 50 ns per division to 5 s per division in 1-2-5 sequence, accurate to 0.1%.

DISPLAY

CRT.

Screen area. 8 x 20 cm.

Graticule. External, 8 x 10 divisions.

Deflection. Electrostatic.

Phosphor. P31.

Characters.

Height. 0.25 cm.

Width. 0.20 cm.

Horizontal spacing. 0.25 cm on centers.

Logic Traces.

Height. 0.5 cm.

Length. 10 cm.

Horizontal resolution. 20 bits/cm.

Time resolution*. 50 ns to 0.2 µs/div -- 10 ns. 0.5 µs/div -- 25 ns. 1 µs to 5 s/div --5X $\frac{s/div}{100}$.

Analog Display Area.

Height. 3.9 cm.

Length. 10 cm.

Vertical resolution. 10 dots/cm, 39 total.

Horizontal resolution. 20 dots/cm, 200 total.

* For trigger position from +7.0 to -90.0 divisions

Sensitivity. 0.5 V/cm to 10 V/cm in 1-2-5 sequence.

Amplitude resolution. 1 part in 39.

MISCELLANEOUS

Memory.

Standard. 4K bytes.

Optional. 16K bytes.

Transcribe.

Records with standard memory. 22 per step, 5 steps maximum.

Records with optional memory. 100 per step.

Size (Excluding Handle).
Height. 8.7 in (22 cm).
Width. 15.7 in (40 cm).
Depth. 18.9 in (48 cm).

Weight (maximum). 48 lbs (22 kg).

Power. 200 W maximum 48 to 62 Hz/100, 120, 200 or 240 ±10%volts RMS /2 A maximum at 100 V.

ACCESSORIES

Data Probe.

Impedance. 10 MΩ, 15 pF.

Attenuation. 10X.

Trigger Probe.

Impedance. 10 MΩ, 15 pF.

Attenuation. 10X.

DATA CARTRIDGE (3M Data cartridge DC100A)

Number of records. 100.

SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model DTO-1.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken knobs and connectors; inspect cabinet and panel surfaces for dents and scratches. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Gould Inc., Biomation Division, representative or the Gould Inc., Biomation Division factory.

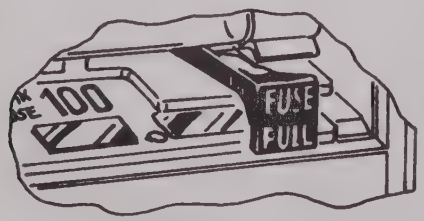
2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Power Connection

CAUTION: Before connecting the unit to AC power, be sure that the proper voltage has been selected.

The operating voltage is shown in the window beneath the fuse clips. See the following sketch.



The Model DTO-1 has a line voltage selector that permits operation at four different nominal line voltages: 100, 120, 220, and 240 VAC. The unit will operate correctly at variations of ± 10% from these nominal voltages, and at line frequencies for 48 to 62 Hz.

To select the operating voltage, perform the following steps.

1. Unplug line cord from rear of instrument.
2. Slide up clear plastic cover and remove fuse using built-in lever.
3. Remove the small circuit board inside the fuse holder using a small hook or screwdriver.
4. Install the circuit board, oriented so that the desired line voltage is visible beneath the fuse clips.
5. Replace the fuse and slide the clear plastic cover over it.

NOTE: When operating at 100 or 120 VAC, use a 2 A slo-blow fuse; at 220 or 240 VAC use a 1 A slo-blow fuse.

Power cable: The Model DTO-1 is equipped with a detachable three-wire power cable. Proceed as follows for installation.

1. Connect line-cord plug (three-socket connector) to AC line jack at rear of instrument.
2. Connect plug (two blades with round grounding pin) to three-wire (grounded) power outlet. Exposed portions of instrument are grounded through the round pin on the plug for safety.

2.5 Preparation for Use

The Model DTO-1 is an integrated, self-contained unit. With its standard accessories (data probe, trigger probe, data cartridge, and power cord) it is capable of performing all the functions covered in the operation section of this manual.

2.6 Initial Warm-Up

Except for the CRT, the Model DTO-1 is a solid-state instrument. Although the instrument is usable after CRT warm-up (approximately one minute), we recommend allowing approximately 10 minutes for the internal circuitry to reach thermal stabli-zation.

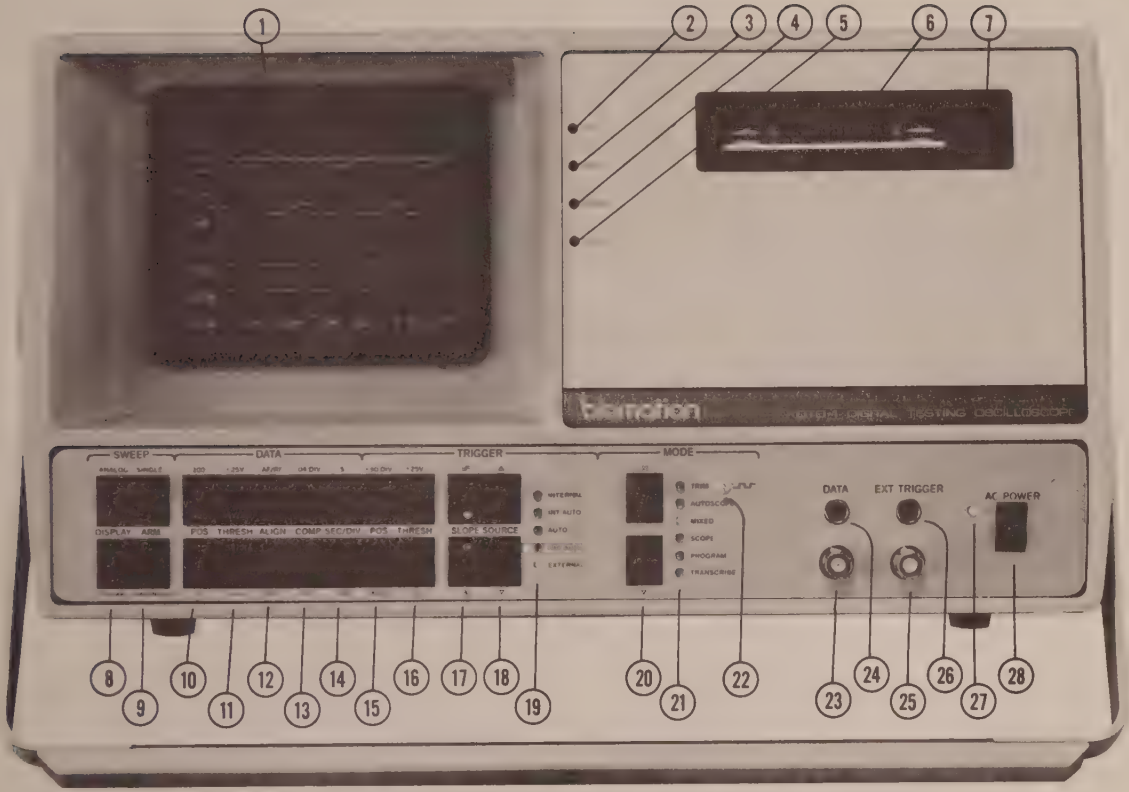


Figure 3.1 Front Panel Functions

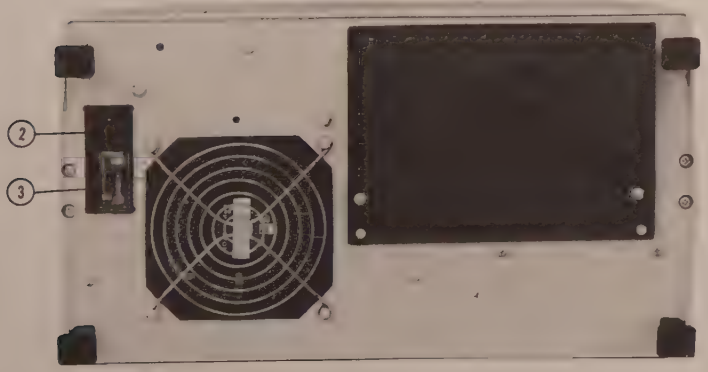


Figure 3.2 Rear Panel Functions

SECTION III

OPERATION

3.1 Introduction

This section identifies and describes front panel, rear panel and probe controls, and provides complete operational procedures.

3.2 Front Panel Controls, Connectors and Indicators

The front panel controls and other features are identified in Figure 3.1 and are described in Table 3.1.

3.3 Rear Panel Controls

The rear panel controls and other features are identified in Figure 3.2 and are described in Table 3.2.

3.4 Data Probe

The data probe controls and indicators are identified in Figure 3.3 and are described in Table 3.3.

3.5 Switches and Nomenclature

The user will quickly become accustomed to the feel and convenience of the pushbutton switches used in the DTO-1.

To understand the five different types of switch responses to momentary, repeated, and continuous depression, the user must first understand the nomenclature associated with the switches.

3.5.1 Nomenclature

The nomenclature between the rows of switches is associated with the nomenclature immediately above and below the switches. The nomenclature engraved on the switches is color keyed for use in certain modes of operation. There are two exceptions to the above. The "FAIL" and "PASS" engraving are only associated with the red and Green LEDs and there is no nomenclature between the mode △ and mode ▽ switches.

3.5.2 Switch Action

The five types of switch action are:

1. SINGLE
   A single or repeated depression, or continuous pressure on a pushbutton produces only a single change.

2. DUAL
   A single depression or continuous pressure on a pushbutton produces a single change of state. Repeated depressions produce an alternation between two states.

3. STEP SEQUENCE
   A single depression or continuous pressure on a pushbutton produces a single change of state. Repeated depressions produce stepping through a number of states until an "end" state is reached at which point repeated depressions produce no change.

4. STEP SEQUENCE, LOOP
   Same as Step 3., except that when "end" state is reached, repeated depressions cause cycle of states to repeat.

5. CONTINUOUS SEQUENCE
   A single depression produces a single step change toward some limit; repeated depressions produce additional step changes toward some limit; continuous pressure produces continuous step changes toward some limit at an increasing rate of change. When a limit is reached, additional depressions have no effect.

Table 3.4 identifies the type of action for each switch.

3.5.3 Switching Sequences

This paragraph describes the switching for switch types 2, 3, 4 and 5 as defined in paragraph 3.5.2 above. The sequences are described in Table 3.5.

Table 3.1 Front Panel Identification and Description

INDEX NO. (Figure 3.1)	NAME	FUNCTION
1	CRT Display	Displays logic traces, analog waveforms, trace numbers, analog voltage scale data threshold, AF/RF ratio, compare tolerance, seconds/division, trigger position, trigger threshold, data error trace, and alphanumerics associated with the transcribe mode and messages to the operator.
2	VERT	Adjusts vertical position of display.
3	HORIZ	Adjusts horizontal position of display.
4	INTENSITY	Adjusts intensity of display.
5	FOCUS	Adjusts focus of display.
6	Receptacle	Receives data tape cartridge.
7	EJECT	Ejects data tape cartridge.
8a	SWEEP,DISPLAY, ANALOG	Displays analog voltage scale and readies unit for acquisition of an analog waveform display.
8b	SWEEP,DISPLAY, CLEAR	In Analog and Trim modes it clears the analog display area. In Autoscope mode it clears trace seven. In Mixed mode it clears trace six. In Scope and Program modes it clears trace 8.
9a	SWEEP, ARM, SINGLE	Arms unit for single sweep in all modes except Transcribe.
	LED	Lights when the unit is armed for single sweep and remains on until the sweep is complete and the trace is displayed.
	YES	Answers "Yes" to questions displayed in the Transcribe mode.
9b	SWEEP, ARM, CONTINUOUS	Automatically rearms unit after each sweep in all modes except Transcribe.
	LED	Lights when the unit is armed or sweeping. It goes off momentarily between sweeps.

Table 3.1 (Con't)

INDEX NO. (Figure 3.1)	NAME	FUNCTION
	NO	Answers "No" to questions displayed in the Transcribed mode.
10a	DATA, POS, 100	Increments the trace numbers toward 100 in all modes except Trim, Analog and Transcribe. In the Transcribe mode it increments the tape record number toward 100.
	+25 V	In the Analog mode it increments the voltage scale toward +25 V. (NOTE: +24 V max at 2 V/cm and +20 V max at 10 V/cm.)
10b	DATA, POS, 1	Decrements the trace numbers toward 1 in all modes except Trim, Analog and Transcribe. In the Transcribe mode it decrements the tape record number toward 1.
	-25 V	In the Analog mode it decrements the voltage scale toward -25 V. (NOTE: -24 V max at 2 V/cm and -20 V max at 10 V/cm.)
11a	DATA, THRESH, +25 V	Increments the data threshold toward +25 V.
	10 V/DIV	In the Analog mode it increases the volts/division toward 10.
11b	DATA, THRESH, -25 V	Decrements the data threshold toward -25 V.
	0.5 V/DIV	In the Analog mode it decreases the volts/division toward 0.5.
12a	DATA, ALIGN, AF/RF	Tells unit to compute and display the AF/RF ratio and to reconstruct and redisplay the reference trace, on line 8, to that ratio. Used only in the Autoscope mode.
12b	DATA, ALIGN, OFF	Turns off Data Align. The AF/RF ratio disappears from the display and the trace on line 8 reverts back to recorded characteristics. Used only in the Autoscope mode.
13a	DATA, COMP, 0.04 DIV	Decreases the allowable disagreement towards 0.04* divisions.
	RED LED	The red LED lights in the Autoscope mode if the amount of continuous disagreement exceeds the compare limit displayed, or if the total disagreement exceeds 30% of the trace.

* These limits apply from 1 μs/div to 5 s/div. Below 1 μs/div the limits are inversely proportional to s/div.

Table 3.1 (Con't)

INDEX NO. (Figure 3.1)	NAME	FUNCTION
13b	DATA, COMP, OFF	Increases the allowable disagreement toward 1.0* division. Continuing past this point will turn the automatic compare mode off.
	GREEN LED	Lights in Autoscope mode if there is a compare limit displayed and if there is no continuous logical disagreement that exceeds that limit, and if the total disagreement does not exceed 30% of the trace.
14a	DATA, SECONDS/ DIVISION, 5	Changes time scale toward 5 s/div.
14b	DATA, SECONDS/ Division, 50 n	Changes time scale toward 50 ns/div.
15a	TRIGGER, POS, +90 DIV	Moves trigger position and displayed traces to the right.** Decreases delay and/or increases pretrigger time of data acquisition.
15b	TRIGGER, POS, -90 DIV	Moves trigger position and displayed traces to the left.** Increases delay and/or decreases pretrigger time of data acquisition.
16a	TRIGGER, THRESH, +25 V	Increases the trigger threshold voltage toward +25 V.
16b	TRIGGER, THRESH, -25 V	Decreases the trigger threshold voltages toward -25 V.
17a	TRIGGER, SLOPE ∫	Sets trigger to positive-going waveform and lights LED.
17b	TRIGGER, SLOPE ⌊	Sets trigger to negative-going waveform and lights LED
18a	TRIGGER, SOURCE △	Changes trigger source toward internal as indicated on adjacent LEDs (Index No. 19).
18b	TRIGGER, SOURCE,▽	Changes trigger source toward external as indicated on adjacent LEDs (Index no 19).
19	Trigger Source LEDs	Indicates the trigger source.
20	MODE △	Changes mode toward TRIM as indicated on LEDs (Index No. 21).

* These limits apply from 1 μs/div to 5 s/div. Below 1 μs/div the limits are inversely proportional to s/div.

** Zero (0.0) trigger position is located at one division from the left of the display. All trigger positions are referenced to this point.

Table 3.1 (Con't)

INDEX NO. (Figure 3.1)	NAME	FUNCTION
20b	MODE ▽	Changes mode toward TRANSCRIBE as indicated on LEDs (Index No. 21).
21	Mode LEDs	Indicates mode of operation.
22	Test Point ⎍⎍	Signal used for compensating probe.
23	DATA, BNC Connector	Data input connector for data probe.
24	DATA, Remote Connector	Provides for hook-up of the remote switches and indicators on the data probe.
25	EXT TRIGGER, BNC Connector	Trigger input connector for trigger probe.
26	EXT TRIGGER Power Connector	Provides power for 10-TC pod.
27	AC POWER, LED	Indicates presence of AC power in the unit.
28	AC POWER, SWITCH	Controls AC power to unit.

Table 3.2 Rear Panel Indentification and Description

INDEX NO. (Figure 3.2)	NAME	FUNCTION
1	Astigmatism Potentiometer	Adjusts display astigmatism.
2	Power Cord Receptacle	AC Power input.
3	Fuse	Protects AC power input.
	Voltage Selection PC Board	Selects AC power line voltage (see Section II, Paragraph 2.4).

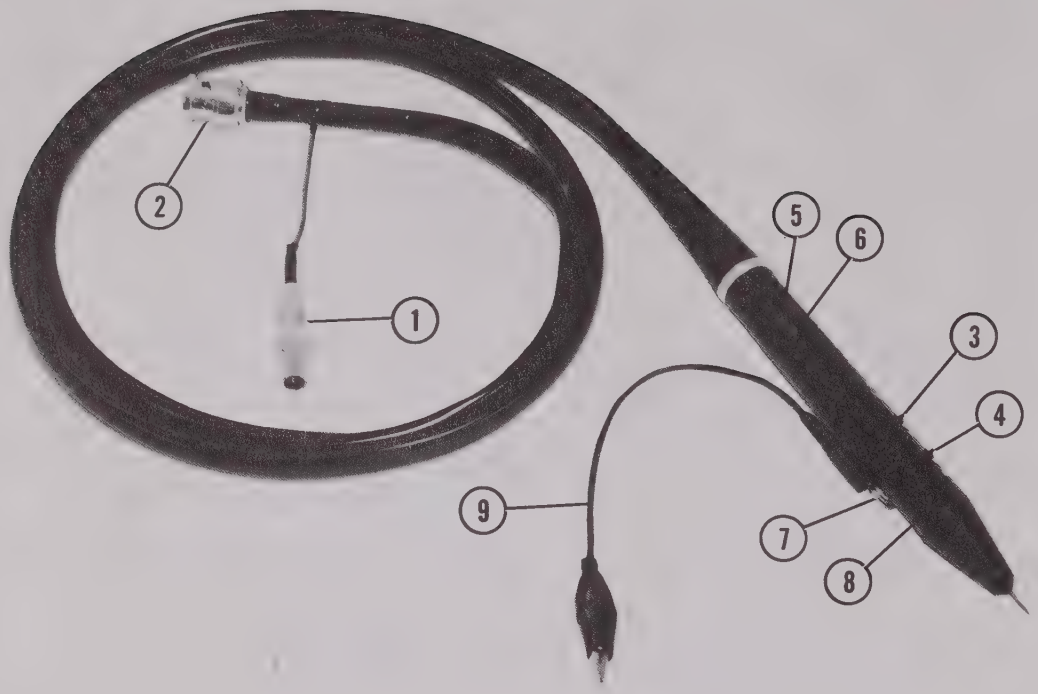


Figure 3.3 Data Probe Functions

Table 3.3 Data Probe Identification and Description

INDEX NO. (Figure 3.3)	NAME	FUNCTION
1	Remote Control Connector	Connects index numbers 3, 4, 5, and 6 to unit.
2	Data, BNC Connector	Connects probe to data input of unit.
3	Advance/Clear Pushbutton	Advances record number in Autoscope, Mixed, Scope and Program modes. Clears analog display in Analog mode.
4	Sweep Pushbutton	Arms unit for single sweeps.
5	LED, Green (2)	Indicates "PASS" condition.
6	LED, Red (2)	Indicates "FAIL" condition.
7	Ground Lug	Provides access to probe ground.
8	Probe adjust	Adjusts probe compensation capacitor.
9	Ground Lead	Connects probe ground to circuit ground.

Table 3.4 Identification of Switch Action

SWITCH	TYPE OF SWITCH ACTION (See Paragraph 3.5.2) 1 SINGLE	2 DUAL	3 STEP	4 STEP,LOOP	5 CONTINUOUS
STANDARD NOMENCLATURE					
DISPLAY ANALOG		X			
DISPLAY CLEAR	X				
ARM SINGLE	X				
ARM CONTINUOUS	X				
POS 100					X
POS 1					X
THRESH +25 V					X
THRESH -25 V					X
ALIGN AF/RF	X				
ALIGN OFF	X				
COMP 0.04 DIV					X
COMP OFF					X
SEC/DIV 5					X
SEC/DIV 50 n					X
POS +90 DIV					X
POS -90 DIV					X
SLOPE ∫	X				
SLOPE ⌇	X				
SOURCE △			X		
SOURCE ▽			X		
MODE △			X		
MODE ▽			X		
COLOR KEYED NOMENCLATURE					
ANALOG +25 V					X
ANALOG -25 V					X
ANALOG 10 V/DIV			X		
ANALOG 0.5 V/DIV			X		
TRANSCRIBE YES	X				
TRANSCRIBE NO				X	
PROBE					
SWEEP	X				
ADVANCE/CLEAR	X				

Table 3.5 Switching Sequences

SWITCH	TYPE (Table 3.4)	SEQUENCE	EXAMPLE
DISPLAY ANALOG	Dual	Switches unit in and out of the analog mode.	Analog Enabled, Analog Disabled, Analog Enabled, etc.
POS 100	Continuous Sequence	Sequentially increments record numbers toward 100.	2, 3---99,100.
POS 1	Continuous Sequence	Sequentially increments record numbers toward 1.	99,98---- 3, 2, 1.
THRESH +25 V	Continuous Sequence	Increments in 0.1 V steps toward +25 V.	-24.9 V, -24.8 V--- +24.9 V, +25 V.
THRESH -25 V	Continuous Sequence	Increments in 0.1 V steps toward -25 V.	+24.9 V, +24.8 V--- -24.9 V, -25 V.
COMP 0.04 Div	Continuous Sequence	Increments in 0.02 div steps toward lower limit.*	(At 1 µs/div) 1.0, 0.98, 0.96----0.06, 0.04.
COMP OFF	Continuous Sequence	Increments in 0.02 div steps toward upper limit* and then to off.	(At 1 µs/div) 0.06, 0.08, ------0.98, 1.0, OFF.
SEC/DIV 5	Continuous Sequence	Increments in 1-2-5 sequence toward 5 s/div.	0.1 µs, 0.2 µs, 0.5 µs, 1 µs, 2 s, 5 s.
SEC/DIV 50 n	Continuous Sequence	Increments in 5-2-1 sequence toward 50 ns/div.	2 s, 1 s, 0.5 s, --- 0.1 µs, 50 ns.
POS +90 DIV	Continuous Sequence	Increments in 0.1 div steps toward +90 div.	--89.9, -89.8- +89.9, +90.
POS -90 DIV	Continuous Sequence	Increments in 0.1 div steps toward -90 div.	+89.9, +89.8-- -89.9, -90.
SOURCE △	Step Sequence	Increments lit LED toward internal.	Ext Auto, Auto, Int Auto, Internal
SOURCE ▽	Step Sequence	Increments lit LED external.	Int Auto, Auto, Ext Auto, External
MODE △	Step Sequence	Increments lit LED toward trim.	Program, Scope, Mixed, Autoscope, Trim.
MODE ▽	Step Sequence	Increments lit LED toward transcribe.	Autoscope, Mixed Scope, Program, Transcribe

* See paragraphs 3.6.1 and 3.9.1.9.

Table 3.5 (con't)

SWITCH	TYPE (Table 3.4)	SEQUENCE	EXAMPLE
ANALOG +25 V	Continuous Sequence	Increments in steps equal to the analog volts/division scale, toward the upper limit.**	(Most positive voltage; 1 V/div) -20 V, -19 V --+24 V, +25 V.
ANALOG -25 V	Continuous Sequence	Increments in steps equal to the analog volts/division scale, toward the lower limit.**	(Most negative voltage; 5 V/div) +5 V, 0 V, -5 V, -10 V, -15 V, -20 V, -25 V.
ANALOG 10 V/DIV	Step Sequence	Increment in 1-2-5 sequence toward 10 V/div.	1 V, 2 V, 5 V, 10 V.
ANALOG 0.5 V/DIV	Step Sequence	Increment in 5-2-1 sequence toward 0.5 V/div.	5 V, 2 V, 1 V, 0.5 V.
TRANSCRIBE NO	Step Sequence Loop	Increments in "read?", "erase?", "test tape?" sequence and then repeats cycle.	Read, Erase, Test Tape, Read, Erase, Etc.

** At 2 V/div, upper limit is +24 V and lower limit is -24 V.
At 10 V/div, upper limit is +20 V and lower limit is -20 V.

3.6 Special Relationships and Limitations

There are special relationships between switch settings that, in certain modes of operation or in certain sequences, do not allow these setting to be changed independently.

3.6.1 Time/Division

In the AUTOSCOPE COMPARE mode, the allowable disagreement is established with reference to a certain time/division. If the SEC/DIV is changed, the compare is changed to maintain the same allowable time limit.

For example, the initial COMPARE setting is 0.04 divisions and the sweep time is 1 µs/division. The compare time is $0.04 \times 1^{-6} = 40$ ns. If the trace is expanded by a factor of two, by changing the sweep time to 0.5 µs/division, the compare setting automatically changes by the same factor to 0.08 divisions. This maintains the established compare time; $0.08 \times 0.5^{-6} = 40$ ns.

3.6.2 Trigger Position

If the trigger position is not set at zero, expanding a trace changes the trigger position relative to the zero trigger reference point by the same ratio that the trace was expanded. Because the trigger position limits are ±90 divisions, no expansion can take place that would put the trigger position beyond these limits.

For example, the trigger position is at -20; sweep time is at 1 µs/cm. The first expansion is to 0.5 µs/cm, an expansion of two times. Two times the position of -20 would be -40. The second expansion would be to 0.2 µs/cm, an expansion of 2.5 or a total expansion of five times. This puts the position at 2.5 X -40 or 5 X -20, which equals 100. Because we cannot exceed -90, the unit does not respond to the second expansion.

3.6.3 Volts/Division

The analog voltage scale naturally changes when the volts per division is changed. However, the volts per division changed cannot be referenced to a particular point on that voltage scale. Therefore, any V/DIV change reestablishes 0 V on the third line from the top of the display. Whenever possible, it is recommended that the volts per division be set first and then analog voltage.

3.6.4 Trace Comparison

In the AUTOSCOPE COMPARE mode of operation it is the intent to compare traces that are acquired under common conditions. That is why the reference trace attributes are recorded on tape and those same attributes are automatically set up when a new trace is to be acquired. As a safeguard against inadvertently comparing traces recorded under different conditions, a new trace cannot be acquired and compared if either the SEC/DIV or POS controls are changed.

3.7 Trigger Modes

There are five trigger modes-Internal, Internal Auto, Auto, External Auto and External. When using the Biomation model 10-TC Probe Pod, there is a sixth "combinational trigger" mode of operation.

The trigger input connector is not used in the internal, internal auto, or auto modes of operation. There is no need, however, to disconnect the trigger probe from a signal when in these modes of operation.

When in the external auto, external, or external with combinational trigger, the trigger probe is connected to the trigger input connectors. When the 10-TC Probe Pod is used, the probe power is obtained through the trigger mini connector just above the trigger input BNC connector.

3.7.1 Internal

In the Internal position, the unit triggers off of the data signal.

3.7.2 Internal Auto

In the Internal Auto position, the unit triggers off of the data signal unless a data signal of sufficient amplitude is not present, in which case the unit triggers automatically.

3.7.3 Auto

In the Auto position, the unit triggers as soon as the unit is armed.

3.7.4 External Auto

In the External Auto position, the unit triggers off of the trigger signal unless a trigger signal of sufficient amplitude is not present, in which case the unit triggers automatically.

3.7.5 External

In the External position, the unit triggers off of the trigger signal.

3.8 Modes of Operation

The following paragraphs briefly describe the purpose of each mode of operation and then what can be done once the unit is in that mode. The step-by-step operating procedures are located in Section 3.9.

3.8.1 Trim Mode

The Trim mode is used to check probe calibration. There is a 0 to +4 V, 1 kHZ squarewave output on the front panel for this purpose. Although all front panel data and trigger switches are operational, they are seldom used in this mode of operation.

3.8.2 Autoscope Mode

The Autoscope mode is used for comparing logic traces. The reference trace from the data cartridge always appears on line eight of the display and the new trace always appears on line seven. All front panel data and trigger switches are operational (see paragraphs 3.6.1 and 3.6.4).

With the compare function off, a visual comparison can be made. With the compare function on, an automatic comparison is made. As long the SEC/DIV is not changed, the compare limits can be changed and still retain the automatic compare feature.

As long as the SEC/DIV is not changed, the align feature can be enabled. The align feature can be disabled at any time.

There can be up to six logic traces on lines one through six. The trace number prefix is either an "A" or an "R" depending

on whether the trace was acquired from the SUT or from tape storage. There is no prefix if there is no trace.

The mixed mode may be entered without losing any of the information displayed on the lower quarter of the CRT.

3.8.3 Mixed Mode

The Mixed mode is entered from the Autoscope mode to retain the logic traces on lines 7 and 8 while looking at other logic traces on lines 1 through 6; while looking at analog waveforms; or while looking at both logic traces and analog waveforms.

The Mixed mode is entered from the Scope mode to retain the logic traces on lines 7 and 8 while looking at other logic traces on lines 1 through 6; or while looking at both logic traces and analog waveforms. Entering the Mixed mode from any other mode simply allows acquisition of logic traces and analog waveforms on lines 1 through 6 with lines 7 and 8 remaining blank.

When in the Mixed mode all data and trigger switches are operational except for the Align and Compare functions. New logic traces are displayed on line 6.

The analog pushbutton must be depressed to display analog waveforms (see paragraph 3.8.5).

3.8.4 Scope Mode

The Scope mode is entered when the DTO-1 is to be used strictly as an oscilloscope or logic analyzer, or when it is desirable to display eight new traces or three new traces with an analog waveform.

When in the Scope mode all data and trigger switches are operational except for the Align and Compare functions.

The analog pushbutton must be depressed to display analog waveforms (see paragraph 3.8.5).

3.8.5 Analog Mode

The Analog mode is entered from the Mixed or Scope modes for the purpose of displaying analog waveforms while retaining up to three logic traces, on lines 6 through 8, from the previous mode.

Any number of analog waveforms may be displayed concurrently in the analog display area as long as none of the displayed attributes are changed between sweeps. Any change of operational data or trigger switch settings clears the analog display area.

The data position and threshold switches become analog voltage switches in the analog mode. All data and trigger switches are operational except for align and compare functions.

3.8.6 Program Mode

The Program mode is used to record logic traces on magnetic tape. A test program is recorded in this mode for recall at a later date in the Autoscope mode. Test programs or historical records of logic traces can be recalled for display in either the Autoscope or Program modes. All data and trigger switches are operational except for the align function.

3.8.7 Transcribe Mode

The Transcribe mode is used to duplicate or reorganize existing tapes, erase magnetic tape records, or verify the correctness of magnetic tapes.

The "Yes", "No", and Data position pushbuttons are the only ones operational in this mode.

3.9 Operating Procedures

3.9.1 General Operating Information

To keep the step-by-step operating procedures as brief as possible, some of the redundant procedural steps, alternate steps, and special operations are treated separately below.

3.9.1.1 Data Align

DATA, ALIGN, AF/RF and OFF pushbuttons can be activated only in the Autoscope mode (see Table 3.1, index numbers 12a and 12b).

Once this function is enabled, it can be disabled only by entering the Trim mode or by depressing the DATA, ALIGN, OFF pushbutton when in the Autoscope mode.

Whenever a test procedure calls for a frequency alignment to be done and there is already an AF/RF ratio displayed, first depress the DATA, ALIGN, OFF pushbutton and then depress and release the DATA, ALIGN, AF/RF pushbutton.

3.9.1.2 Indexing Tapes

There are two methods for indexing a blank tape.

1. Enter the Program mode and insert tape.

2. Enter the Transcribe mode and ask the instrument to erase number 001-100. (See paragraph 3.9.2.6, steps 1 and 11-15.)

3.9.1.3 Probe and Ground Connections

Prior to acquisition of any signal:

1. Connect data probe ground lead to system under test.

2. Whenever using External Trigger mode of operation, be sure to connect trigger probe and trigger probe ground lead to the system under test.

3.9.1.4 Data Probe ARM, ADVANCE pushbuttons

In writing the step-by-step operating procedures, a standard X10 data probe was used with the DTO-1. When using the special data probe with ARM and ADV pushbuttons, the following procedure changes can be made.

1. The probe ARM pushbutton can be used wherever the SWEEP, ARM, SINGLE pushbutton is called out.

2. The probe ADV pushbutton can be used wherever the DATA, POS, 100 pushbutton is called out.

3. The probe ADV pushbutton can be used to clear the display when in the Analog mode of operation.

3.9.1.5 Clearing the Display

Analog Waveforms - In the Trim, Mixed/Analog and Scope/Analog modes of operation, newly acquired signals will be superimposed on any existing waveforms unless the display is first cleared.

Logic Traces - There is no need to clear the display prior to acquisition of a new signal. The displayed trace will automatically be cleared prior to display of a new trace.

3.9.1.6 Continuous Sweep

The Continuous Sweep mode can be used anytime SWEEP, ARM, SINGLE is called out; however, it is probably most useful in the Mixed or Scope mode during troubleshooting procedures.

Continuous sweep is obtained by depressing the SWEEP, ARM, CONTINUOUS pushbutton. There are two ways to disable the continuous sweep function.

1. Depress the CLEAR pushbutton until the LED on the continuous switch goes off. The appropriate display area will be cleared.

2. Depress the SWEEP, ARM, SINGLE pushbutton until the LED on the continuous switch goes off. Sweeping will stop at the end of the next complete sweep. None of the displayed information will be cleared.

NOTE: No control settings can be changed during continuous sweep.

3.9.1.7 Changing the Control Settings

The control settings can be changed at anytime with the following exceptions:

1. As stated elsewhere in Section III of this manual.

2. While the instrument is carrying out a prior instruction.

3.9.1.8 Data Error Trace

In the Autoscope mode, the logic trace from the system under test is being compared

with the logic trace from the known good system. The exact areas of disagreement are underscored on the display. This underscoring is present whether or not the automatic compare (COMP) function is being used. It gives the operator a quick and accurate visual indication of where the disagreements are located.

The data error trace is expanded or compressed along with the logic traces when the time base is changed. It is also retained when going from the Autoscope to the Mixed mode.

3.9.1.9 Data Compare (COMP)

The compare limit, in display divisions, is one of the controls set up in the Program mode. (See Table 3.1, index number 13a and 13b.) In the Autoscope mode, this is the limit that sets the pass/fail indicators. It does this by comparing the data error trace against this limit. (See Table 3.1, index numbers 13a and 13b.)

The compare limit can be changed in the Autoscope mode.

The smallest compare limit that can be set is the larger of 0.04 divisions or the number of divisions representing 4 sampling bits of the internal clock. In all cases where the latter would be the larger of the two, the internal clock would be 100 MHz and the sampling interval would be 10 ns. Therefore, the compare limit cannot represent less than 40 ns. It follows that automatic comparisons connot be made to limits of less than 40 ns.

However, using a sweep time of 50 ns/DIV, a visual comparison can be made with a resolution of 10 ns and typical accuracy of 20 ns.

3.9.1.10 PASS/FAIL LEDs

Prior to acquisiton of a trace in the Autoscope mode, the read LED will be lit. This is a ready indication, or to put it another way, the operator is to take some action. Shoot a trace!

The read (FAIL) indication after acquisition of a signal also tells the operator to take action. In this case he should look at the display.

If no trace appears on line 8 in the Autoscope mode, the green LED will be lit. (You might say that nothing is being compared against nothing.) In this case the unit cannot be armed.

When there is a trace on line 7 and the COMP function is off, neither the red LED or the green LED will be lit.

The pass/fail LEDs operate only in the Autoscope mode except as noted in paragraph 3.9.1.11.

3.9.1.11 Self Test

Each time the unit is powered up or enters the Trim mode, it self-tests the major portions of the device including the MPU, firmware RAMs. If the microprocessor is unable to access the ROM or RAM, both the pass and the fail LEDs will become lit. The defective device can be located using Table 3.6 and Figure 3.4.

3.9.1.12 Offset Errors

If "OFFSET ERROR" is displayed, it means that the dc offset of the input circuitry exceeds 50 mV. If this should occur, depress the clear pushbutton and then proceed. The instrument will automatically calibrate itself to eliminate the offset.

3.9.1.13 Tape Errors and Dirty Heads

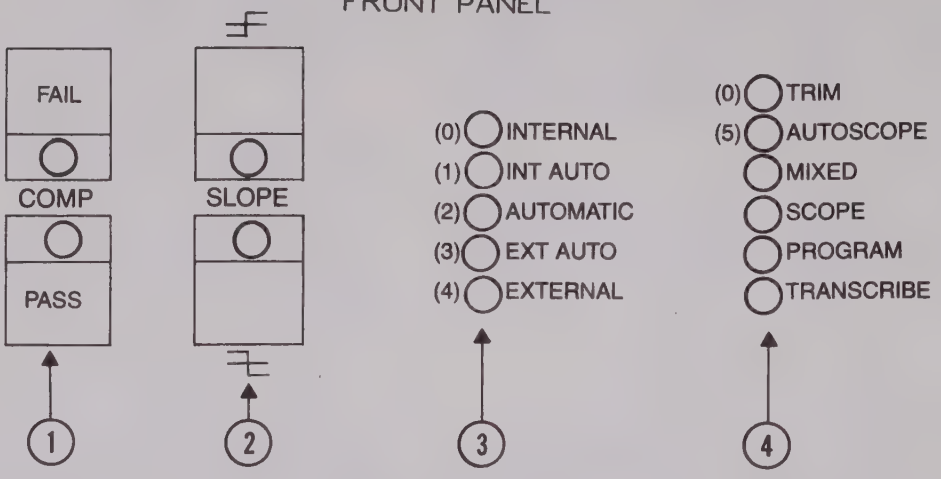
If any of the following messages appear on the display, you either have a dirty read/write head or a tape problem.

"READ or WRITE ERROR"
"READ ERROR at ***"
"INDEX ERROR"
"INDEX ERROR at ***"

Cleaning the head will usually solve a nonrepetitive type problem. If a read error repeats at a specific record, that record will have to be reprogrammed. If an index error repeats at a specific location, that record must be worked around or the entire tape must be reindexed and refreshed from your master tape.

In the Autoscope mode, an error can be worked around by depressing the CLEAR pushbutton and then proceeding. An "E" will be displayed in front of the record number containing the error.

Table 3.6 Self Test - Diagnostic Error Identification



Both the PASS and FAIL LEDs (1) will light when there is a failure in the memory access routine.

One of the SLOPE LEDs (2) will light. The upper LED, ⊣F , indicates that the failure is in one of the eight ROMs. The lower LED, F⊢ , indicates that the failure is in one of the eight RAMs.

The weighted TRIGGER LEDs (3) and MODE LEDs (4) locate the defective chip. Add the weight, in parenthesis, of the one LED lit at (3) to the weight of the one LED (TRIM or AUTOSCOPE) lit at (4). Locate the chip using the control board layout Figure 3.4.
(NOTE: The sum will not exceed 7.)

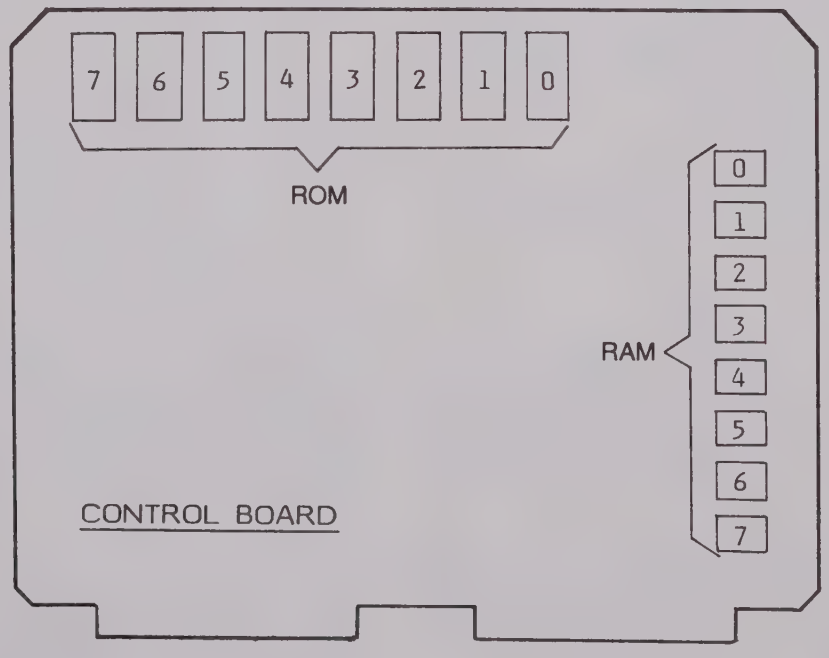


Figure 3.4

3.9.2 Step-by-step Operating Procedures

3.9.2.1 Trim Mode

STEP	PROCEDURE	INDICATION
1	Enter the TRIM mode.	A voltage scale will appear on the left side of the display and controls will be automatically set for acquisition of the probe calibration waveform.
2	Hold probe to be calibrated to the TRIM terminal. Press and release the SWEEP, ARM, SINGLE pushbutton.	Calibration signal will be displayed.
3	Adjust probe compensation capacitor if required.	
4	Press and release the CLEAR pushbutton.	Displayed signal is cleared.
5	Repeat steps 2, 3 and 4 until probe is properly compensated.	

3.9.2.2 Autoscope Mode

STEP	PROCEDURE	INDICATION
1	Insert prerecorded data cartridge and enter the AUTOSCOPE mode.	From two to seven index or record numbers will be displayed on the left side of the CRT. The numerical part of the number on line 8 will be duplicated on line 7. For those record numbers that have a logic trace recording on tape, an "R" prefix will appear in front of the record number. The records are numbered consecutively from top to bottom except for the duplication on lines 7 and 8. The control settings are displayed across the bottom of the CRT and on the front panel LEDs. The control settings will be those of the trace on line 8. If no trace appears on line 8, the most recently used settings will be displayed. The data align AF/RF ratio will normally be off when starting a new test sequence. (See Paragraph 3.9.1.1).
2	Place desired record number on line 8 of the display using the DATA, POS pushbuttons.	Desired logic signal appears on line 8. The controls will automatically be set for the trace on line 8.
3	Connect trigger probe and ground leads as required.	
4	Probe the test point that corresponds to the record number on line 8.	
5	Press and release the SWEEP, ARM, SINGLE pushbutton.	A logic signal will appear on line 7. An "A" will appear in front of the record number on line 7. The green, PASS, or the red, FAIL, LED will become lit. The "Data Error Trace" will appear immediately below the logic signal on line 7 if there is any logical disagreement between the traces on lines 7 and 8.

STEP	PROCEDURE	INDICATION
6	If no frequency alignment is to be done, proceed to step 7. If a frequency alignment is to be done (see paragraph 3.9.1.1), depress and release the DATA, ALIGN, AF/RF pushbutton.	The AF/RF ratio appeared on the display. The trace on line 8 was cleared from the display and then reappeared after being aligned to the clock or reference signal of the system under test.
7	If there was a "PASS" condition in the last step, the test is complete. Additional tests can be made by repeating steps 2-7. If there was a "FAIL" condition in the last step, either proceed to a preprogrammed subroutine, or enter the MIXED mode for manual trouble-shooting (See paragraph 3.9.2.3 Mixed Mode.)	

STEP	PROCEDURE	INDICATION
1	Enter the MIXED mode.	The trace number 001 will appear on line 6. Logic traces, if any, on lines 7 and 8, and control settings, will be holdovers from the previous mode.
3	Probe test point. Depress and release the SWEEP, ARM, SINGLE push-button.	A logic signal will appear on line 6. An "X" will appear in front of the trace number.
4	If the logic signal on line 6 is to be retained and a new logic signal is to be displayed, depress and release the DATA, POS, 100 pushbutton.	The trace number and trace move up to line 5 and the next consecutive number appears on line 6.
5	Repeat steps 2, 3 and 4 for each new logic signal to be displayed.	Same as above except in step 4 all traces above line 6 will move up one position and the trace on line 1, if any, will be lost.
6	If the analog waveform of the input signal is to be displayed, depress and release the ANALOG pushbutton.	The traces, if any, on lines 1 through 5 will disappear from the display. A voltage scale will appear on the left side of the display.
7	Probe test point. Depress and release the SWEEP, ARM, SINGLE push-button.	An analog waveform will be displayed. (NOTE: Probe must be held to the test point until complete waveform is displayed.)
8	To superimpose additional analog waveforms on the display, repeat step 7.	Additional waveforms will be super-imposed on the existing waveforms.
9	If new analog waveforms are to be displayed by themselves, depress the CLEAR pushbutton. Repeat step 7.	The analog waveform will disappear from the display. Same as step 7.
10	To disable the analog function, depress and release the ANALOG pushbutton.	The voltage scale and analog wave-forms will disappear from the display. Any logic traces that were present on lines 1 through 5 prior to entering the analog mode will reappear. The control settings will remain as they were in the analog mode.

STEP	PROCEDURE	INDICATION
11	In order to return to the autoscope mode, depress and release the MODE pushbutton.	Lines 1 through 6 will clear. Logic traces, if any, that were present on lines 1 through 6 prior to entering the mixed mode will be displayed, except that "A" traces will be replaced by "R" traces recalled from tape. Control settings will be recalled from tape for the trace on line 8.
12	In order to return to the scope mode, depress and release the MODE pushbutton.	Lines 1 through 6 will clear. Trace numbers, if any, that were present on lines 1 through 6 prior to entering the mixed mode will be displayed without prefixes or traces. Control settings will not change.

STEP	PROCEDURE	INDICATION
1	Enter scope mode.	Display is clear except for the trace number 001 and controls settings. Control settings are holdovers from previous mode.
2	Probe test point. Depress and release the SWEEP, ARM, SINGLE pushbutton.	A logic trace will appear on line 8 and the prefix "S" will be added to the trace number.
3	If additional signals are to be displayed, depress and release the DATA, POS, 100 pushbutton.	The logic trace and trace number will move up to line 7 and the next consecutive number will appear on line 8.
4	Repeat steps 2 and 3 for each new signal that is to be displayed.	Same as above except that in step 3, all logic traces and trace numbers will move up one position. As traces move off the top of the display they will be lost.
5	If the analog waveform of an input signal is to be displayed, depress and release the ANALOG pushbutton.	Lines 1 through 5 of the display will be cleared. A voltage scale will appear on the left side of the display.
6	Probe the test point. Depress and release the SWEEP, ARM, SINGLE pushbutton.	An analog waveform will be displayed.
7	To superimpose additional analog signals on the display, repeat step 6.	Additional waveforms will be displayed.
8	To clear the display prior to acquisition of new analog signals, depress the CLEAR pushbutton.	The analog waveform(s) will be cleared.
	Repeat step 6.	Same as step 6.
9	To disable the analog mode, depress and release the ANALOG pushbutton.	Lines 1 through 5 of the display will be cleared. Any logic traces and trace numbers that were present on lines 1 through 5 prior to entering the analog mode will be displayed.

STEP	PROCEDURE	INDICATION
1	Enter the PROGRAM mode and insert the data cartridge. NOTE: IT IS EXTREMELY IMPORTANT TO OBSERVE THE TRIGGER MODE LED DURING THE COURSE OF PROGRAMMING A TAPE. UNLESS A PREVIOUS PROGRAM HAS BEEN ERASED, THE TRIGGER INFORMATION FROM THAT PROGRAM MAY CHANGE YOUR INTENDED SETTING AND GO UNDETECTED. (SEE PARAGRAPH **** FOR PROGRAMMING NOTES.) WHEN USING AN EXTERNAL TRIGGER, BE SURE THAT IT IS PROPERLY SELECTED. SHOULD THERE BE ANY DOUBT, DISPLAY THE LOGIC TRACE SEVERAL TIMES AND CHECK FOR REPEATABILITY BEFORE PUTTING IT IN TAPE STORAGE.	a) **Using unindexed tape.** The statement "INDEXING TAPE - WAIT 60 SEC" will appear on the display. When indexing is complete, the index numbers 093-100 will appear along the left side of the display. The most recently used control settings will appear across the bottom of the display and on the trigger slope and trigger source LEDs. b) **Using pre-indexed tape.** From one to eight consecutive index or "record" numbers will appear along the left side of the display. Where there is a logic signal stored on tape, the record number will have an "R" prefix. The stored signal, if any, may or may not be displayed as logic traces depending on the SEC/DIV and Trigger POS control settings. The control settings will be displayed across the bottom of the display and on the Trigger slope and Trigger source LEDs. The control settings will be those of the trace on line 8. If no trace is displayed on line 8, the most recently used settings will be displayed.
2	Using the DATA, POS pushbuttons, position the desired record number on line 8 of the display.	If a record position change was made, see step 1b above.
3	Set controls and connect ground leads and trigger probe as required.	
4	Probe test point. Depress and release the SWEEP, ARM, SINGLE pushbutton.	A logic trace will appear on line 8 of the display. The prefix "P" will appear in front of the record number on line 8. ("P" indicates it is a proposed trace.)
5	If the logic trace displayed is to be recorded on tape, proceed to step 6. If any change is made to the control settings, reacquire the logic trace before proceeding to step 6.	

STEP	PROCEDURE	INDICATION
6	Depress and release the DATA, POS, 100 pushbutton.	All displayed record numbers and traces moved up one division on the display. The prefix on the trace just recorded changed from "P" to "R". ("R" indicates that the trace has been recorded on tape.) The next consecutive number will appear on line 8. If there is a trace displayed on line 8, and if the SEC/DIV and TRIGGER, POS control settings have changed, the traces on lines 1 through 7 will be redisplayed to agree in both time and position with the new settings.
7	To record additional signals, repeat steps 2 through 6.	

STEP	PROCEDURE	INDICATION
1	Enter the transcribe mode. NOTE: BEFORE STARTING ANY PROCEDURE TO TRANSCRIBE RECORDS ON TO A NEW TAPE, BE SURE THAT YOUR NEW TAPES HAVE BEEN INDEXED. METHODS FOR INDEXING CAN BE FOUND IN PARAGRAPH 3.9.1.2.	"READ 001?" appears on the display.
2	If the "Erase" operation is to be performed, proceed to step 11. If the "Test Tape" operation is to be performed, proceed to step 17. If records are to be transcribed to another tape or to a new position on the same tape, proceed to step 3.	
3	If the lowest record number to be transcribed is 001, proceed to step 4. If the lowest record number to be transcribed is not 001, use the DATA, POS pushbuttons to display the lowest number that is to be transcribed.	The number selected (XXX) will appear on the display. (READ XXX?)
4	Depress and release the "YES" pushbutton.	"READ XXX - XXX?" appears on the display.
5	If only a single record is to be transcribed, proceed to step 6. If a block of records is to be transcribed, use the DATA, POS pushbuttons to display the highest consecutive record number that is to be transcribed.	The number selected (YYY) will appear on the display. (READ XXX - YYY?)
6	Depress and release the "YES" pushbutton.	"READING - WAIT" will appear on the display. Then "WRITE XXX - YYY to XXX -YYY" will be displayed.

STEP	PROCEDURE	INDICATION
7	If the records are to be written onto a new tape at the same location, proceed to step 8. If the records are to be written to a new location, either on the same tape or on a new tape, use the DATA, POS pushbuttons to select the block of consecutive numbers at the new location.	The block of numbers selected (WWW - ZZZ) will appear on the display. (WRITE XXX - YYY to WWW-ZZZ?)
8	If the records are to be moved to a new location on the same tape, proceed to step 9. If the records are to be transcribed to another tape, remove the data cartridge and insert the other pre-indexed data cartridge.	
9	Depress and release the "YES" push-button.	The tape will move to the first record in the group to be transcribed. "WRITING-WAIT" will then appear on the display. When the writing is complete, "WRITE XXX-YYY to WWW-ZZZ again?" will appear on the display.
10	If the records transcribed in step 9 are to be recorded on additional tapes, repeat steps 8 and 9. This completes the transcribe procedure.	
11	Depress and release the "NO" push-button.	"ERASE 001?" appears on the display.
12	If the lowest record number to be erased is 001, proceed to step 13. If the lowest record number to be erased is not 001, use the DATA, POS pushbuttons to display the lowest number that is to be erased.	The number selected (XXX) will appear on the display (ERASE XXX?)
13	Depress and release the "YES" push-button.	"ERASE XXX-XXX?" will be displayed.

STEP	PROCEDURE	INDICATION
14	If only a single record is to be erased, proceed to step 15. If more than one consecutive record is to be erased, use the DATA, POS pushbuttons to display the highest consecutive number that is to be erased.	The number selected (YYY) will be displayed. (ERASE XXX-YYY?)
15	Depress and release the "YES" pushbutton.	The tape will move to the first record to be erased. "ERASING -WAIT" will then appear on the display. When the records have been erased, "ERASE XXX-YYY AGAIN?" will be displayed. NOTE: If the entire tape is being erased, records 001-100, instead of displaying "ERASING - WAIT", "INDEXING TAPE - WAIT 60 SEC." will appear. After erasure is complete, "ERASE 001-100?" will be displayed.
16	If additional tapes are to have the same records erased, remove the tape just erased and insert the next tape to be erased. Repeat step 15. This completes the erase procedure.	
17	Depress and release the "NO pushbutton.	"ERASE 001?" will be displayed.
18	Depress and release the "NO" pushbutton.	"TEST TAPE?" will be displayed.
19	Depress and release the "YES" pushbutton.	"TESTING - WAIT" will be displayed. After testing, "TEST TAPE AGAIN?" will be displayed.
20	If additional tapes are to be tested, remove the tape just tested and insert the next tape to be tested. Repeat step 19.	

SECTION IV

PRINCIPLES OF OPERATION

4.1 Introduction

This section provides a basic functional description and a detailed circuit description of the DTO-1.

4.2 Basic Functional Description

For the discussion that follows, refer to the block diagram, Figure 4.1.

4.2.1 Front Panel Boards

Front panel and data probe switch information is made available to the Control board. The data and trigger settings are then stored in RAM.

Instrument status information from the Control board is displayed via front panel and data probe LEDs.

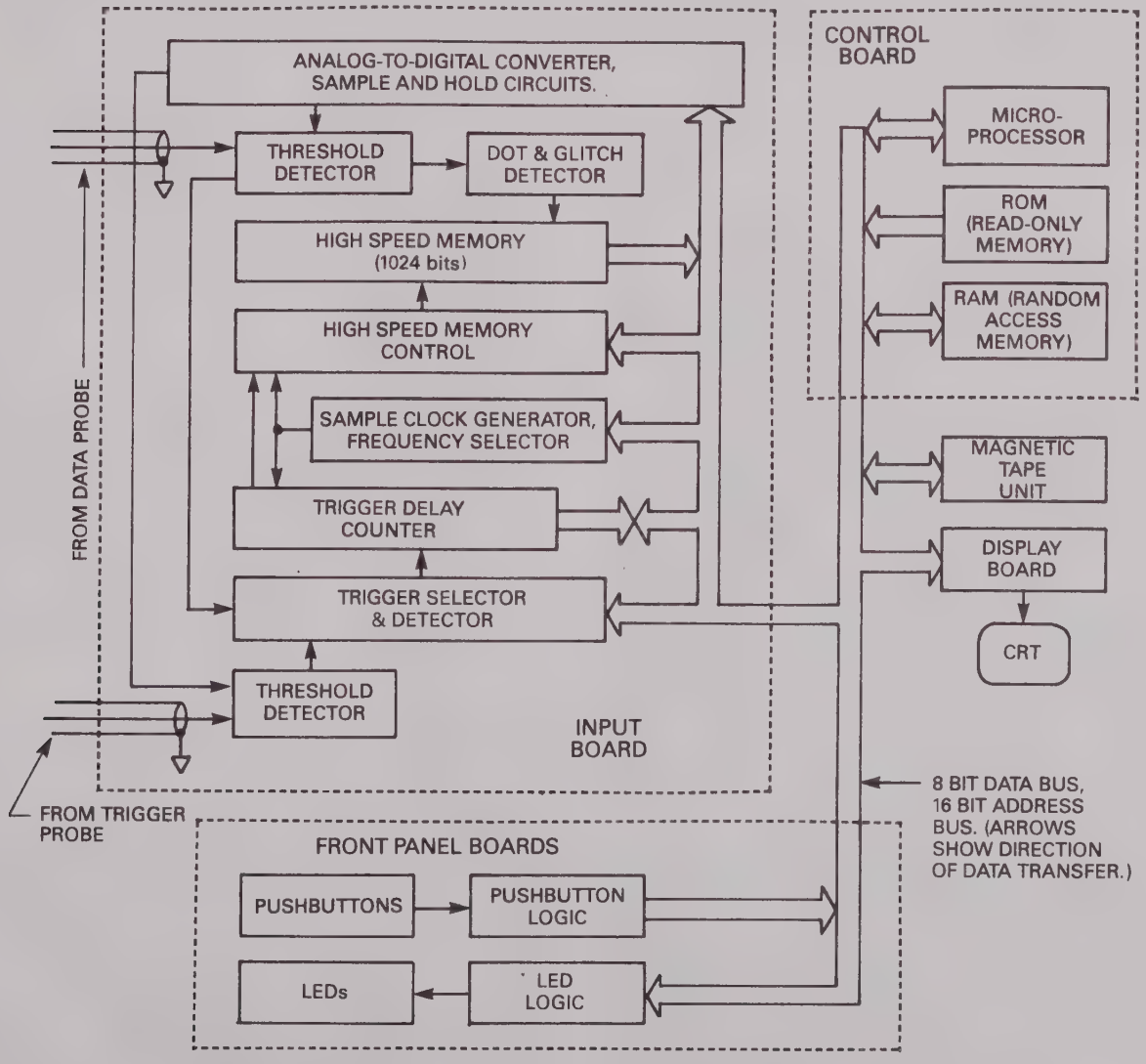


Figure 4.1 DTO-1 Block Diagram

4.2.2 Control Board

The Control board controls all operations directly or indirectly performed by the DTO-1. Front panel switches read by the Control board are translated into the control signals required to perform the assigned task. The Control board contains a Motorola 6800 microprocessor, Read Only Memory (ROM), Read-Write Memory (RAM), and a Direct Memory Access (DMA) controller, all connected together by an address and data bus and synchronized by a timing generator.

4.2.3 Display Board

Data representing the information to be displayed on the CRT is stored in the microprocessor RAM. The Display board reads this data through the DMA channel and converts it to three analog signals for the CRT display unit.

4.2.4 Input Board

The input board is, in essence, a variable speed analog-to-digital converter. The Analog Input signal is converted to a digital data stream that is stored in memory. The Data or External Trigger input can identify when the conversion is to take place.

Before the input signal can be digitized, the Input board must be initialized by setting the sample clock frequency, the trigger delay counter, the trigger source, the mode "analog" or "digital", and the input threshold voltages. The microprocessor controls these circuit functions by writing data into latches and counters on the Input board. The microprocessor can also test the results of processes by reading the status of the Input board.

4.2.5 Signal Acquisition, Storage and Display

Signal acquisition is accomplished by sampling the input at rates up to 100 MHz. For logic recording, a string of "1's" and "0's", relative to the data threshold level, are continually stored in a 1024-bit high-speed memory. When a trigger event occurs and a trigger event countdown is complete, the 1024-bit high-speed memory is halted and the most recently stored 1000 bits are transferred to a low-speed RAM area.

High speed analog waveform recording is handled in a similar manner except that the process is repeated 39 times, looking at different threshold levels or windows on each pass. The high-speed memory again stores 1024 bits for each scan and transfers this information to RAM. Closely spaced threshold voltages are established for each scan with a logic "1" recorded only if the input is within that window during the associated sampling interval. After 39 scans, bits describing the complete waveform reside in RAM.

For low-speed analog waveform recording, only one occurrence of the signal is required. A successive approximation digitization is made during each sampling interval, and the appropriate column of the 39 row by 200 column memory matrix is developed.

The stored data, for both logic and analog recordings, includes the control settings at which those recordings were made. This data is continually read by the display circuitry to provide X, Y and Z signals to the CRT where the logic traces and waveforms appear.

A logic trace always consists of 200 display bits. Depending upon the SEC/DIV and TRIGGER POSITION settings, anywhere from 40 to 1000 of the 1000 stored bits are used to make up the display bits. Whenever the number of stored bits to be displayed exceeds the number of display bits (200), an algorithm is used to process the stored bits in such a manner that a change of state during any display interval will always be detected and displayed.

Once a logic trace is in RAM and displayed, it can be transferred to tape storage. This can be accomplished only in the PROGRAM mode and only for the most recently acquired logic trace. Except for the bit transfer in and out of the high-speed memory, all other data transfers are in bytes; i.e., RAM to display, RAM to tape, tape to RAM.

Each displayed logic trace is stored in RAM twice. Once as it was originally acquired and once as it is displayed. The 1000 bits in the first location never change, while the display bits in the second location

change as the display parameters are changed; i.e., SEC/DIV, TRIGGER POSITION, AUTO ALIGN.

When the automatic align feature is enabled, the AF/RF ratio must be determined. This is accomplished by counting the total number of bits between the first and last transition for the total number of complete cycles recorded. The total number of bits is divided by the number of complete cycles to yield the number of bits per cycle. Doing this for both the "A" and "R" traces yeilds the frequency ratio.

The number of display bits per cycle of the "R" trace is then increased or decreased to agree with the number of bits per cycle of the "A" trace.

In the automatic COMPARE mode, the bits stored in RAM for both the "A" and "R" logic traces are compared bit by bit. Where there is logical agreement, there will be a "O" logic level, and a disagreement will produce a logic "1". This data is stored in RAM and is displayed as an underscoring of the "A" trace. Only the logic "1" bits are intensified and, therefore, visible on the display.

Another function of the processor is to take these logic "1" areas of disagreement and make a PASS/FAIL decision. It compares the number of consecutive errors against the allowable predetermined limit. If the consecutive errors exceed this limit, the FAIL LED is lit. If the total number of error bits exceeds 30% of the recorded bits, there will also be a FAIL indication. If neither of these limits is exceeded, the PASS LED is lit.

In storing a record on magnetic tape, the 1000 logic bits, the associated 120 control setting bits, and the 8-bit CRC (cyclic redundancy check) are automatically recorded twice in succession. The CRC is a hamming code obtained when the complete string of 1120 bits is divided by a nine term polynomial.

When reading a record, the record index number (1 to 100) is first verified, then the first group of 1120 bits is read into RAM. If a CRC byte developed as described above agrees with the CRC byte from magnetic tape, the 1120 bits are retained in RAM.

If the first of the two test-record copies fails the CRC, the second is read and checked. If both fail, these redundant checks are made up to three more times by rewinding and rereading the two records.

If all eight CRCs fail, the microprocessor displays the message READ ERROR AT XXX (the record index number). Pressing the clear button results in the trace being displayed with an E instead of its normal R prefix.

4.3 Detailed Description

This part of Section IV gives a detailed, circuit-by-circuit description of the Model DTO-1.

4.3.1 Front Panel Circuitry

The Front Panel circuitry performs three functions. It displays instrument status information via LEDs, sends control switch information to the processor, and couples switch and pass-fail information to the probe.

The processor controls all front panel operations through the Data Bus, Address Bus and the WP signal, which originate on the Control board. To illuminate one or more LEDs, the processor addresses either U6 or U7 by setting either A0 or A1, and puts the appropriate information on the data bus and pulses WP high. The low levels from the data bus are latched into U6 to light the PASS, FAIL, ARM SINGLE, ARM CONTINUOUS, TRIGGER SLOPE or TRIGGER SLOPE as required. A 3-bit binary code latched into U7 1Q, 2Q and 3Q selects one of the mode LEDs through U8. Also a 3-bit code on U7 4Q, 5Q and 6Q selects one of the trigger source LEDs through U9. To determine if one of the panel switches is depressed, the processor selects one of the four banks of switches by the binary code of A0, A1 acting through gates U4-6, U4-3, U4-11 or U4-8 to bring the switch commons low. If a switch is closed, a low level is coupled through U1 to the data bus when the processor brings RP low. If one of the Data Input Probe switches is depressed, a low level is coupled through U5-3 and Q2 or U5-11 and Q1 to U1.

The Pass and Fail lights on the Data Input Probe are turned on by either a positive or negative current into the reverse con-

nected LED pairs. To turn on the Pass LEDs, a low is latched into U6-1Q (as before for the panel Pass LED) turning on Q3 and Q4. Q4 conducts current from ground in the probe through the two green LEDs to-5.2 V. To turn on the probe Fail LEDs, a low is latched into U6-2Q turning Q5 on. Q5 conducts currents from +5 V through the red LEDs in the probe.

4.3.2 Input Board

The Input board is, in essence, a variable speed analog-to-digital converter. The Analog Input signal is converted to a digital data stream that is stored in memory. The Data or External Trigger input can identify when the conversion is to take place. Refer to Figure 4.2, block diagram, before reading the following detailed description.

4.3.2.1 Initialization

Before the input signal can be digitized, the Input board must be initialized by setting the sample clock frequency, the trigger delay counter, the trigger source, the mode "analog" or "digital", and the input threshold voltages. The microprocessor controls these circuit functions by writing data into latches and counters on the Input board. The microprocessor can also test the results of processes by reading the status of the Input board. Refer to Table 4.1 for the signals under the control of the microprocessor.

The 100 MHz oscillator (7K-15) is divided by decades to 10 Hz. One of the decade frequencies is selected by SCA, SCB and SCC through multiplexer 8J. The output of 8J is further divided by two and five by

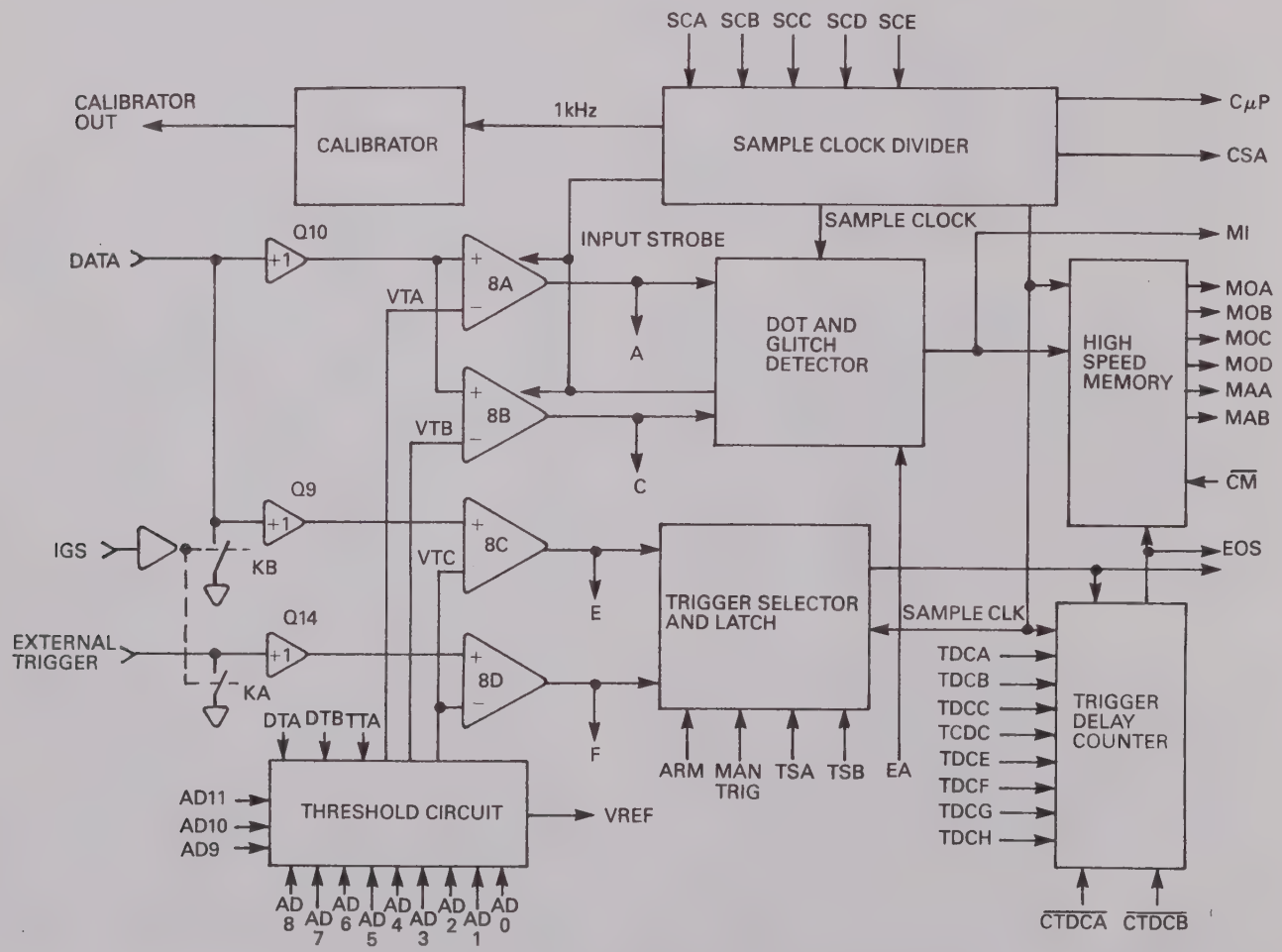


Figure 4.2 Input Board Block Digram

Table 4.1 Signals Under Control of the Microprocessor

Write	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	-	-	AD5	AD4	AD3	AD2	AD1	AD0
1	0	0	1	-	-	AD11	AD10	AD9	AD8	AD7	AD6 TTL
2	0	1	0	-	-	-	-	IGS	TTA	DTB	DTA
3	0	1	1	-	-	EA	SCE	SCD	SCC	SCB	SCA
4	1	0	0	-	-	-	MAN TRIG	ARM	-	TSB	TSA
5	1	0	1	TDC7	TDC6	TDC5	TDC4	TDC3	TDC2	TDC1	TDC0 (CTDC A)
6	1	1	0	TDC15	TDC14	TDC13	TDC12	TDC11	TDC10	TDC9	TDC8 (CTDC B)
7	1	1	1	*	*	*	*	*	*	*	* ($\overline{CM}$)

* The high speed memory is clocked independent of the data.

READ	A3	A2	A1	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	A	-	MAB	MAA	MOD	MOC	MOB	MOA
1	0	0	1	C	-	MAB	MAA	MOD	MOC	MOB	MOA
2	0	1	0	E	-	MAB	MAA	MOD	MOC	MOB	MOA
3	0	1	1	F	-	MAB	MAA	MOD	MOC	MOB	MOA
4	1	0	0	T	-	MAB	MAA	MOD	MOC	MOB	MOA
5	1	0	1	EOS	-	MAB	MAA	MOD	MOC	MOB	MOA
6	1	1	0	$\overline{CSA}$	-	MAB	MAA	MOD	MOC	MOB	MOA
7	1	1	1	MI	-	MAB	MAA	MOD	MOC	MOB	MOA

7H. SCD and SCE select either the undivided output or the output divided by two or five. The selected frequency at the common output of 7F is the sample clock frequency and is delayed and buffered by 8F-2 and 7E for use throughout the Input board.

The trigger delay counter 3F, 4F, 3E, and 4E is preset with the 16-bit complement of the number of sample clock pulses to be counted after the trigger event. The data bus, buffered by 3H and 4H and shifted to ECL levels, is clocked into 3F and 4F by $\overline{\text{CTDCA}}$ and into 3E and 4E by $\overline{\text{CTDCB}}$.

The trigger source, one of the four outputs of 8C and 8D, is selected by TSA and TSB through multiplexer 7D to the clock of 6D-15. The trigger source is thus selected as either the positive or negative slope of the DATA or EXTERNAL TRIGGER input.

Input data may be taken in any one of four ways depending on the front panel controls.

1. High Frequency Digital
2. Low Frequency Digital
3. High Frequency Analog
4. Low Frequency Analog

If an Analog mode is selected, the Dot and Glitch detector is configured to detect Dots by E_A; otherwise, E_A is set low, configuring the Dot and Glitch detector to detect glitches. In both Analog modes, with E_A high comparators 8A and 8B are strobed by the sample clock. In the Digital modes the comparator outputs are active at all times.

The threshold voltages required by the comparators as references for detecting the input signals are established by the microprocessor. Before setting the threshold voltages, the offsets of the input amplifiers Q9, Q10 and Q14, and of the comparators are measured by the processor through the threshold circuit. To measure the offsets the microprocessor sets IGS high, grounding the Data and Trigger Inputs through KA and KB. The microprocessor then determines the voltage required at VTA, VTB and VTC to produce a change of level at comparator outputs A, C, and E or F. If one of the inputs requires more than $\pm$50 mV, the corresponding input is not calibrated and one or more "INPUT OFFSET ERROR" messages will show on the CRT. With the offsets determined, the microprocessors adjust the voltages set at VTA, VTB and VTC to one-tenth of the required threshold voltages.

The threshold circuit consists of +10 V reference 10E, registers 11H and 10H, digital-to-analog converter 11F, output amplifier 11E, three switch 10D holding capacitors C13, 19 and 25, and amplifiers 10B, 10A and 10C. During a measurement the microprocessor automatically controls the DAC inputs and switches to maintain the required threshold voltage VTA, VTB, and VTC.

With DTA, DTB and TTA low, the processor loads registers 10H and 11H with the binary value of the voltage to be set as threshold voltage VTA. The output of digital-to-analog converter 11F is a current proportional to the binary input. Amplifier 11E produces a voltage proportional to the 11F output current that, when acting through resistors internal to 11F between 11F 10 and 11F 9 and 11, hold pins 11E-8, 9, and 11 at ground. Table 4.2 shows the expected output voltage at 11E-6 for selected binary inputs to 11F.

After the voltage at 11E-6 has stabilized, DTA is set high turning on CMOS switch 10D-3,4. Capacitor C13 charges to the desired threshold voltage until DTA is set back low and the switch opens. In a similar manner, voltages VTB and VTC are set and held on capacitors C19 and C25.

The process of repeatedly charging capacitors C13, 19 and 23 maintains the required threshold voltages stable at the inputs to unity gain buffer amplifiers 10B, 10A and 10C. The outputs of the unity gain buffers are filtered to remove any high frequency noise, presenting clean, stable, and accurate threshold voltages to the inputs of the comparators.

Comparators 8A through 8D compare the reference voltages on their negative (-) input to the buffered Data or External Trigger inputs. When the Data or External Inputs are more positive than the corresponding reference voltage, an ECL high level is present on pin 7.

Table 4.2
Selected Digital-To-Analog Output Voltages

AD												Output Voltage
11	10	9	8	7	6	5	4	3	2	1	0	11 E-6
0	0	0	0	0	0	0	0	0	0	0	0	-2.56000
0	1	1	1	1	1	1	1	1	1	1	1	-0.00125
1	0	0	0	0	0	0	0	0	0	0	0	0.00000
1	0	0	0	0	0	0	0	0	0	0	1	+0.00125
1	1	1	1	1	1	1	1	1	1	1	1	+2.55875

The incoming signal is processed by the DTO-1 in one of four ways depending on the front panel control settings. The processing is dependent on the sample clock frequency and whether an analog or digital trace is to be displayed. The four conditions are shown in Table 4.3.

The most common mode of signal processing is High Speed Digital. To initiate the recording of a digital trace, the SWEEP ARM SINGLE or SWEEP ARM CONTINUOUS is depressed and the processor initializes the input circuitry as described previously. The processor then sets ARM (9J-10) high so that data prior to a trigger event can be loaded into memory.

In the digital recording modes the threshold voltage at 8A-3 and 8B-3 are separated by 20 mV to provide hysteresis. Whenever the input signal at 8A-2 is more positive than the upper threshold level at 8A-3, 6B-2 is set. Whenever the input signal at 8B-2 is less positive than the lower threshold voltage at 8B-3, 6B-2 is reset.

Brief pulses or glitches either momentarily high or low occurring between rising edges of the clock are latched into 6B-2 if the output of 6B-2 and 6B-15 are the opposite state of the glitch. As an example, suppose the signal had been less positive than the threshold voltage for several clock cycles causing 6B-2 and 6B-15 to be low. If the signal becomes more positive than the threshold for more than 10 ns, 6B-2 is preset high by 6A-2. Then, regardless of the sample clock frequency, the high state on 6B-2 is clocked into 6B-15 and then into the high speed memory. A negative-going glitch after being high resets 6B-2 through 6A-15 and is latched

Table 4.3

Processing Method	Sample Clock Frequency	Seconds/Division*
Low Speed Digital	20 Hz to 500 Hz	0.5 to 5
High Speed Digital	1 kHz to 100 MHz	50 ns to 0.1
Low Speed Analog	100 Hz or 200 Hz	0.5 to 5
High Speed Analog	500 Hz to 100 MHz	50 ns to 0.2

*Assumes trigger position < +7.1 divisions.

into 6B-15 on the next rising edge of the clock. A continuous series of glitches produces alternating highs and lows from the glitch detector indicating that a noisy input signal or too low a sample frequency has been selected. With E_A low the $\overline{Q}$ output 6B-15 is gated through 5C-2 to the Dot and Glitch Detector output register 5D-2, which is also clocked by the sample clock. The output of the Dot and Glitch Detector is connected to the High Speed Memory.

The active high and active low data inputs to the High Speed Memory are translated from ECL to TTL levels by 4C-4 and 4C-5. The sample clock is divided by 2D-2 and 2D-15 to form a four phase clock for the memories. These four ECL level clocks are translated to TTL by 1D. Because the TTL memories 1B, 1F, 2B and 2F cannot store data at 100 MHz, the data stream is demultiplexed into four separate memories, each with its own address counter and input register. The clock phases and timing for memory 1B are shown in Figure 4.3, timing diagram.

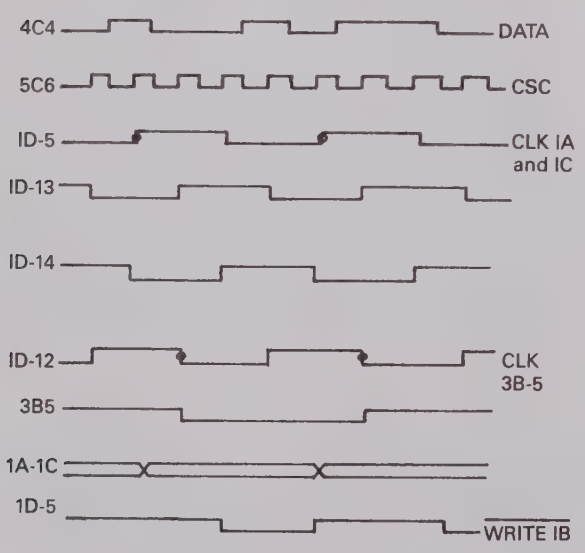


Figure 4.3 High Speed Memory Timing Diagram

Because the memory address counters and clock register 2D are not preset prior to accepting new data, the data is stored sequentially until the trigger event occurs and the Trigger Delay counter stops the high speed memory. Then the data is clocked out of the memory in the same sequence as it was entered. This is possible because the address counter repeats the same address sequence every 256 clocks regardless of where they start. The first, fifth and ninth data bits are clocked into 3B-9 then stored in successive addresses of 2B; the second, sixth, and tenth bits are clocked into register 3C-5 then stored in successive addresses of 2F; the third, seventh, and eleventh bits are clocked into 3B-5 then stored in 1B and so forth until the required pretrigger data has been stored in memory.

Low Speed Digital traces are detected in the same manner as High Speed Digital traces through the input amplifiers, comparators, and the Dot and Glitch Detector; however, the high speed memory is not used. To permit the trace data to be displayed on the CRT as it is being recorded, the processor monitors the sample clock signal through multiplexer 6C-13 and transfers the data directly to the processor memory from the output of the Dot and Glitch Detector at 5D-2.

4.3.2.2 Input Amplifier Circuits

The External Trigger and Data Inputs are coupled to the DTO-1 through X10 probes similar to conventional oscilloscope probes. The signal is attenuated by the ratio of the 9 MΩ resistor in the probes and the 1 MΩ resistors (R50 and R82) in the DTO-1. The variable capacitors in the probe compensate the probe cable and DTO-1 input capacitances. Diodes CR1, CR2, CR3 and CR4 clamp any out-of-range input signals to plus and minus 3 V to prevent damage to the DTO-1 input circuitry. Resistors R46 and R80 limit current into the protection diodes. FET matched pairs Q10, 9, and 14 form unity gain voltage amplifiers with low output impedances to drive the voltage comparators. Two amplifiers are used on the Data Input to isolate the data and trigger comparator circuits so that trigger comparator noise doesn't degrade the signal to the data comparators 8A and 8B.

High Speed Analog signals are recorded using a unique 1-bit conversion technique (patent application pending). At the start of the conversion, threshold VTA is set to a voltage equal to the highest voltage to be displayed on the CRT and VTB is set to a

voltage one-tenth of a division lower. At the falling edge of CS a 2 ns pulse briefly enables comparators 8A and 8B. If the DATA INPUT signal is more positive than the threshold voltages, the comparator outputs latch high; if the DATA INPUT is more negative than VTA or VTB one of the corresponding outputs latches low. The output of 8A is latched into register 6B-2 and the output of 3B is latched into register 6B-15 on the rising edge at the sample clock. Gate circuitry 5B-3, 5B-15, 5B-2 and 5C-15 output a high level to latch 5D-2 only if the signal was between or has just crossed the threshold voltages. Data from the Dot and Glitch Detector is clocked into the High Speed Memory just as it is in the High Speed Digital mode. After the trigger event and count down have occurred, the data indicating when the signal was in the first "window" is transferred from the high speed memory to the processor memory. Threshold voltage VTA is then decreased by two-tenths of a division creating a new window and new data. The windows are leapfrogged down and data is transferred to the processor memory until 39 200-bit lines are stored in the processor memory. These 39 200-bit lines of data are used to intensify dots on the CRT screen to produce the High Speed Analog Display.

A Low Speed Analog Display is recorded by a successive approximation routine. Rather than requiring 39 repetitions of a low speed analog signal, the waveform is digitized completely as it occurs. After each rising edge of the sample clock, the processor digitizes the signal according to the routine shown in Figure 4.4.

The Threshold voltage is initialized to the mid-value of the analog display area, the raster number (R) is set to 20 (equivalent to

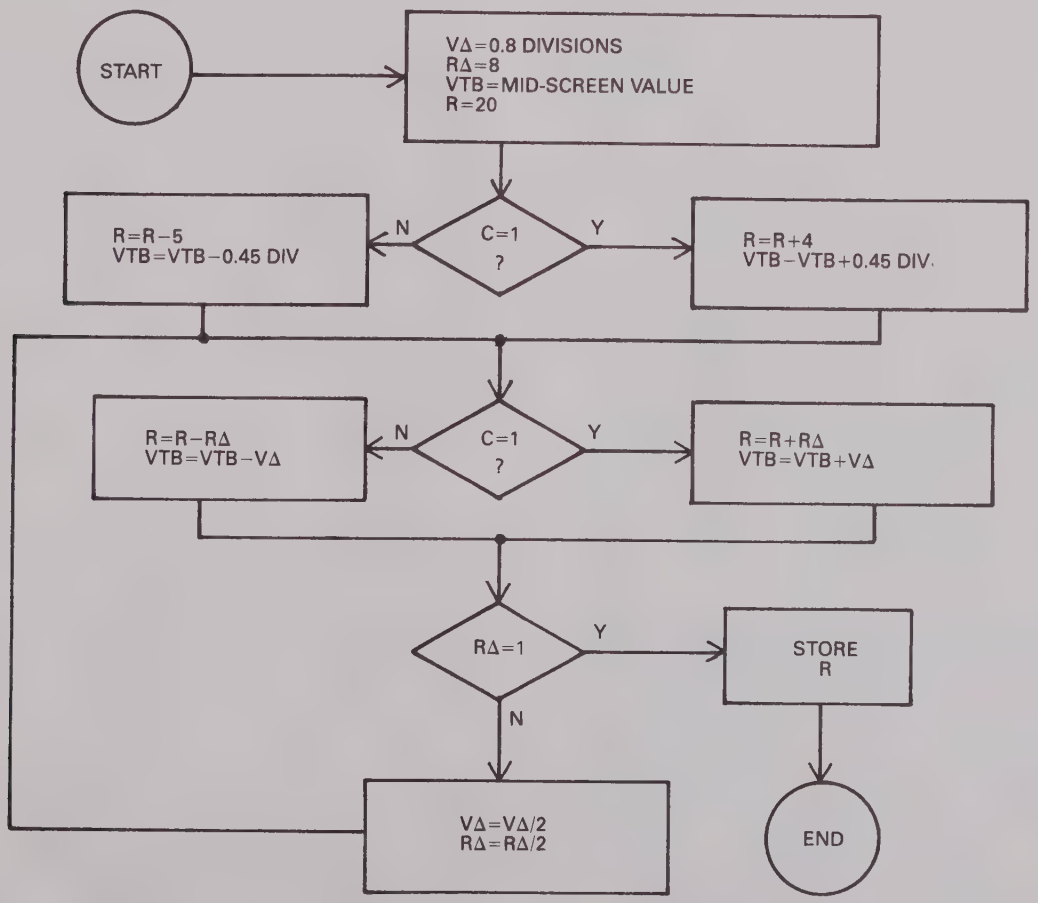


Figure 4.4 Diagram of Low Speed Analog Conversion

the mid-value), the change in raster is set to 8 and the change in VTB (VA) is set to 0.8 divisions. The first decision about C (the output of 8B) determines if the signal is above or below the mid-value, then adjusts R and VTB accordingly. The second decision is made four times, each time adjusting VTB and R toward the signal value and the dot position to be intensified on the display. When the C=1? decision has been made the last time, the value of R is stored in the processor memory. After digitization is complete, the processor fills in the rising and falling edges of any vertical discontinuities in the displayed waveform. Signal frequencies higher than one-fourth the sample frequency can cause erroneous displays.

4.3.2.3 Trigger Circuit

The recording of a trace while initiated by a high ARM signal, is terminated by the Trigger Circuit. After sufficient pretrigger data has been recorded, the processor sets ARM low, then recording continues until a trigger occurs and the trigger delay counter counts up to FFFF HEX. The trigger event can come from either the DATA INPUT, the EXTERNAL TRIGGER or the processor. The EXTERNAL TRIGGER is attenuated to one-tenth its actual value by the 9 MΩ input resistor of the probe and the 1 MΩ resistor R82 in the DTO. The resulting signal is buffered by Q14 so that it can drive the comparator circuit. The (-) input to comparator 8D is threshold voltage VTC and the (+) input is the attenuated and buffered EXTERNAL TRIGGER voltage. If the EXTERNAL TRIGGER is selected, TSB is high enabling 8D outputs 7 and 8.

If a positive slope, external trigger is selected 8D-7 is connected through 7D to 6D-11. When a positive transition with respect to the threshold voltage occurs, flip-flop 6D-15 is set. A small portion of the output of comparators 8C and 8D are fed back to the (+) inputs of 8C and 8D to prevent oscillations. Negative slope transitions are coupled through 7D and 8D-8. Internal triggers are obtained from the DATA INPUT through buffer Q9 and comparator 8C in a similar manner to external triggers. After 6D-15 is set, the trigger is recognized on the next rising edge of CS by 6D-2. When 6D-3 goes low, gates 6E-3 and 6E-2 are enabled and the sample clock begins incrementing the Trigger Delay Counter. When the Trigger Delay Counter reaches its top count (FFFF), 3D-3 goes high and on the next sample clock 5D-15 goes high, stopping the High Speed Memory by inhibiting 5E-2. The processor detects the end of the recording process by testing EOS at 6C-12.

After EOS, the processor transfers the contents of the high speed memory to the processor memory. Memory outputs MAA and MAB identify which of the memory data outputs MOA, MOB, MOC or MOD is active at each location. The processor identifies the first bit, reads it, writes it into the processor memory, then advances to the next High Speed Memory location by bringing $\overline{CM}$ (3J7) low momentarily. This process is repeated until all the required bits have been transferred.

4.3.3 Display Board

Refer to the back diagram in Figure 4.5. Data representing the information to be displayed on the CRT is stored in the microprocessor RAM. The Display board reads this data through the DMA channel and converts it to three analog signals for the Model 350 CRT display unit. The X output controls the horizontal position of the electron beam, the Y output controls the vertical position of the electron beam, and the Z output controls whether the beam is turned on or off. By modulating the X, Y, and Z signals, the display board paints a new picture on the CRT 50 times per second.

The Display board sequences through three display modes during each display cycle. The three modes are Digital Trace, Analog Trace and Character Display. When power is first applied to the DTO, $\overline{POP}$ is low and the circuit is reset; when $\overline{POP}$ returns high the Digital Trace mode is entered.

Each mode is indicated by a flip-flop. During the Digital Trace mode, T (2E-6) is high; during the Analog Trace mode, A (2E-9) is high; during the Character Display mode, W (2F-9) is high. When trace descriptions or characters are being transferred through the DMA channel from RAM, M (3F-9) is high. Figure 4.6 shows the time relationships of these signals.

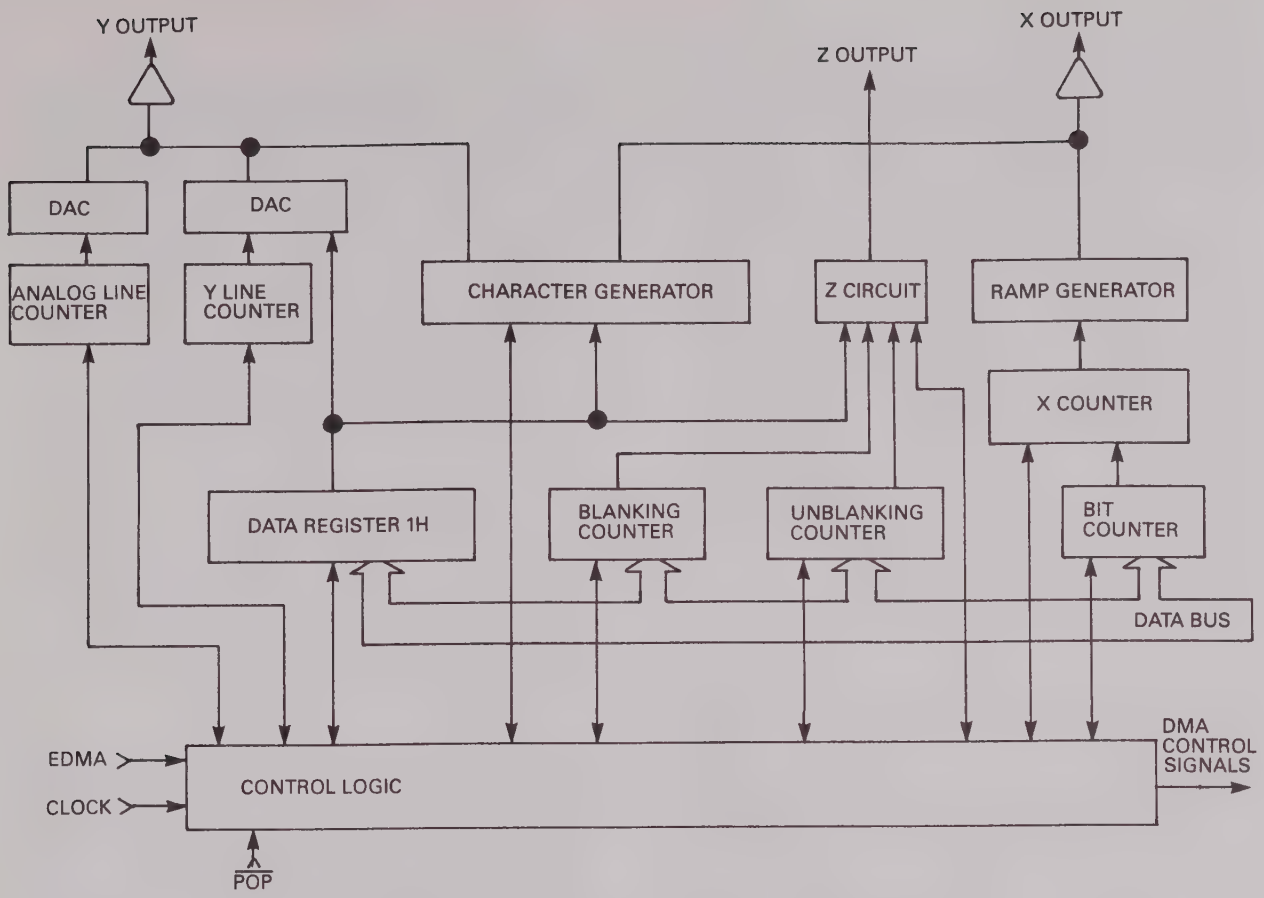


Figure 4.5 Display Board Block Diagram

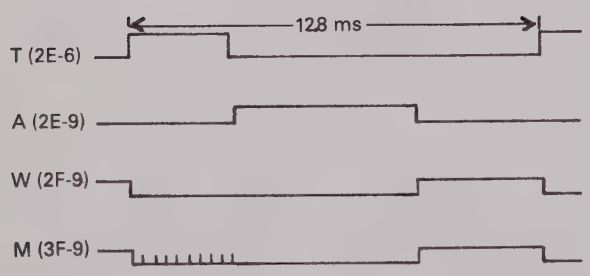


Figure 4.6 Signal Time Relationships

To display the first trace at the top of the CRT, the DMA channel is activated and the unblanking, blanking, and data location are read from RAM. Unblanking time is loaded into 2K and 3K, banking time is loaded into 4K and 5K and the starting bit location is loaded into 1K. The start word and page locations are loaded into the 12-bit DMA address counter on the Control board. The first word of trace data is read from the RAM address indicated by the 12-bit DMA address counter. The data is transferred from RAM via the data bus to 1H. The data bits in 1H are scanned by counter 1E and multiplexer 1F, but the X sweep is not enabled until the start bit is reached as indicated by 1K. When the last bit in the first data word has been displayed, the DMA channel reads the next memory location into 1H and each bit is read. As each bit is read the unblanking and blanking counters are incremented. When the unblanking counter reaches all ones, the beam is turned on. When the blanking counter reaches all ones, the beam is turned off. As the data bits are read the X counter 6D and 6E is incremented.

The data multiplexed through 1F-5 modulates the Y output to produce the high-low logic diagram. As the X counter is counting up, the ramp generator is enabled and current source Q17 charges C39 producing a linear voltage ramp at 8J-6. The Y digital signals, including the Y line counter input, are converted to an analog level by 7J to produce the voltage step necessary for the Y output. At the end of the digital trace the X counter is reset, the X ramp is reset, the Y line counter is incremented, a new trace description is obtained from RAM and the whole process is repeated until the eighth trace. During the eighth trace the data modulates the Z output rather than the Y to underline the seventh trace as required. After the eighth trace the bottom trace is developed as usual.

During the second display mode, the analog trace, if any, is displayed. After the Digital Trace mode is completed, the Display board picks up the Analog Trace description. The blanking word is loaded into 4K and 5K and blanks the analog trace completely unless the word is all one's. The unblanking word is loaded into 2K and 3K but is not used. The address of the first word of trace data is loaded into the 12- bit DMA address counter on the Control board. The Y output is set down one division, the analog line counter 6F and 6G is set to 1, the X ramp is reset, and the X counter is reset. The first data word is accessed from RAM and loaded into 1H. The X ramp and X counters are enabled and each bit of the data word is read in sequence through the multiplexer to intensify modulate the beam. When the 200 bits of the 25 data words have been read and the X counter reaches 200, the beam is turned off, the X ramp is reset and the Y output is moved down one-tenth of a division. When the X counter reaches 208, it is reset to 1 and the next line of data is displayed. After 39 lines of data the analog line counter indicates the end of the Analog Display mode.

During the third display mode, the characters and symbols (see Table 4.4) are written on the CRT. Each character is read in sequence from the RAM address indicated by the 8-bit address counter on the Control board and stored in 1H. The Y line counter and DAC position the beam for the first character.

The 32-word character generator ROM 1G is addressed by the word in 1H. The output 1G controls the stroke circuit. the ROM output can cause the spot on the CRT to move in any one of eight directions with the beam on and any one of seven directions with the beam off, or reset the beam to its point of origin. Once the character is loaded into 1H, counter 1E, 1C-6, 1C-9 addresses in sequence the 32 strokes to make the required character or symbol. After the last stroke (S31) the beam is positioned to the next origin by the X ramp generator and Y counter and DAC.

Table 4.4 Display Words and Symbols

00_H	"BLANK"	08	8	10	P	18	?
01	1	09	9	11	R	19	+
02	2	0A	0	12	S	1A	-
03	3	0B	A	13	T	1B	C
04	4	0C	E	14	W	1C	D
05	5	0D	G	15	u	1D	.
06	6	0E	I	16	n	1E	F
07	7	0F	N	17	m	1F	X

Four characters or symbols are generated in the first division of the first seven lines and forty on the bottom line. If the most significant bit of the word in 1H is a one the character or symbol is shifted down 3/32 of a division.

4.3.4 Control Board

The Control board controls all operations directly or indirectly performed by the DTO-1. Front panel switches read by the Control board are translated into the control signals required to perform the assigned task. The Control board contains a microprocessor, Read Only Memory (ROM), Read-Write Memory (RAM), and a Direct Memory Access (DMA) controller, all connected together by an address and data bus and synchronized by a timing generator. Refer to the block diagram in Figure 4.7.

4.3.4.1 Timing Generator

The Timing Generator breaks the 1 μs system cycle into several time intervals. Each 1 μs interval is divided so that it shares the RAM between the DMA Channel and the microprocessor.

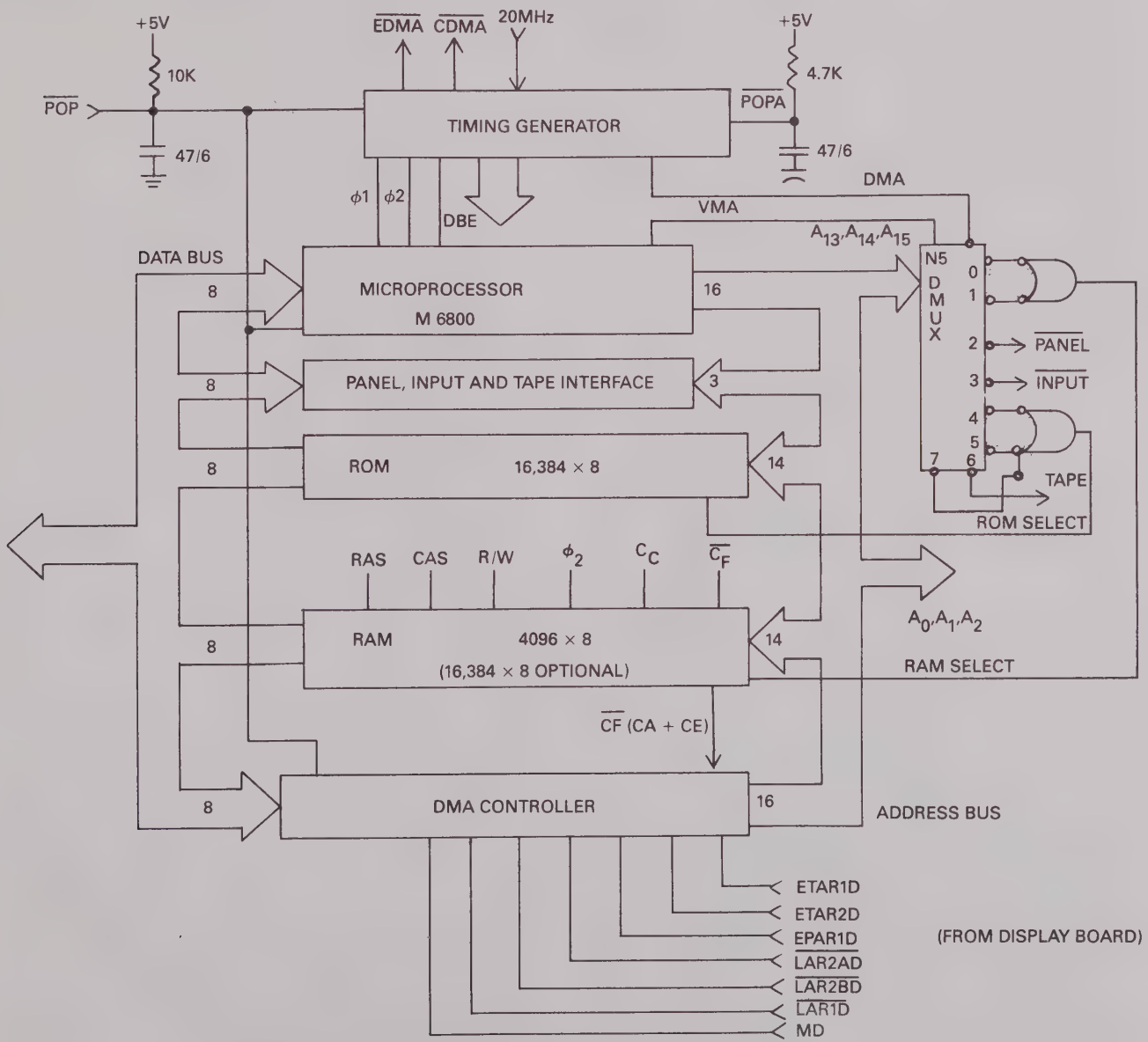


Figure 4.7 Control Board Block Diagram

When power is applied to the system flip-flops H2-5, H2-9, L2-5, L2-9, L3-5 and L3-9 are reset to zeroes during the R15, C42 charging time constant. Then the 20 MHz Clock from the Input board increments the 20 state feedback register H2-5 through L3-5 and toggles L3-9, dividing each 1 μs into 20 states. Refer to the timing diagram in Figure 4.8.

The following signals are derived from this counter:

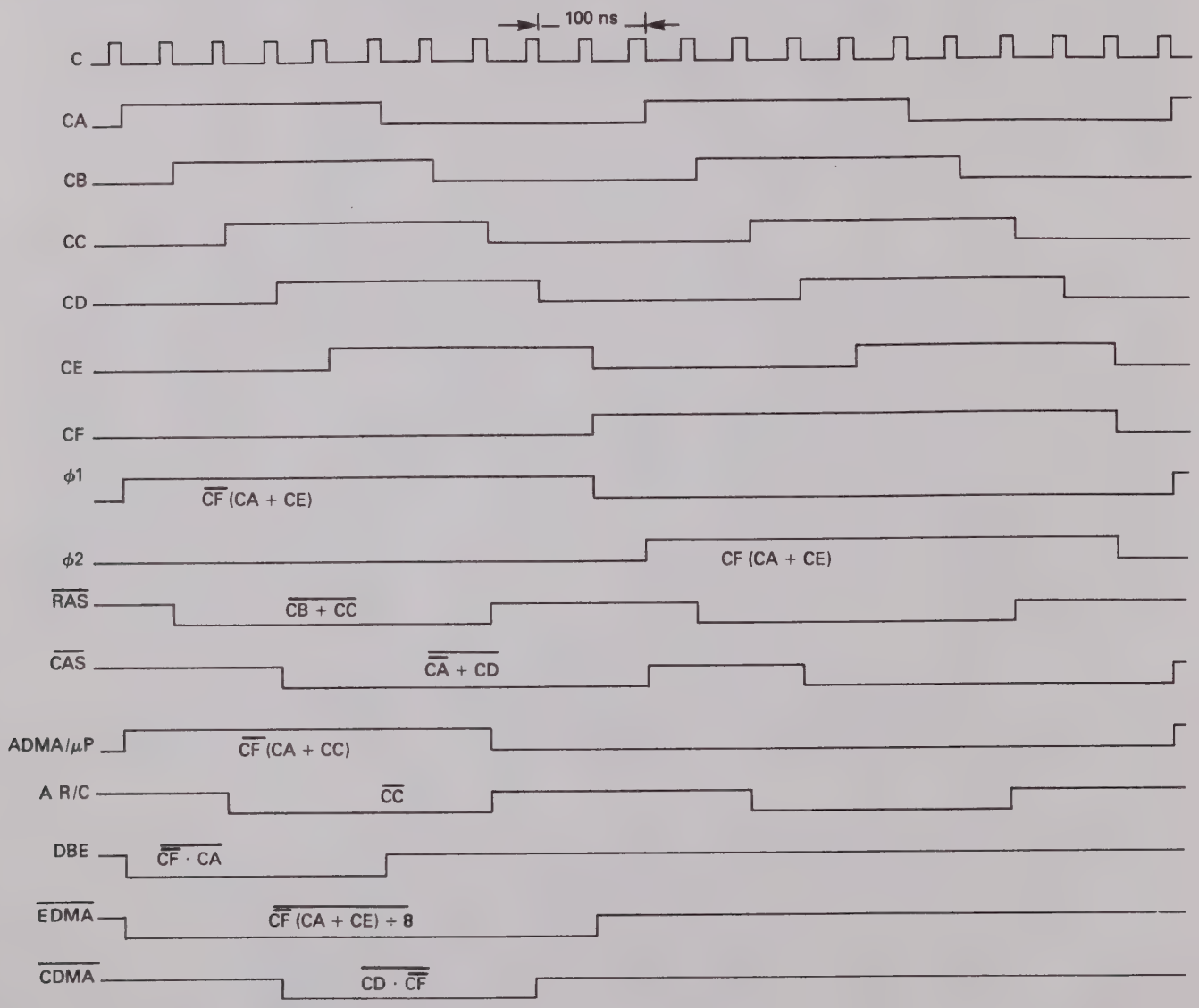


Figure 4.8 Cycle Sharing Timing Diagram

A. Microprocessor

1.	Ø1 Clock	H4-11
2.	Ø2 Clock	H4-8
3.	DBE	H4-3

B. RAM

1.	$\overline{RAS}$	N11-8
2.	$\overline{CAS}$	N11-10
3.	$\overline{WRITE}$	H1-8
4.	$\overline{ROE}$	N11-6
5.	CC	L2-5
6.	$\overline{CC}$	L2-6

C. Data Bus Control

1.	CF	L3-9

D. DMA

1.	$\overline{EDMA}$	H3-12
2.	$\overline{CDMA}$	E4-11

Counter N4 gates EDMA so that it occurs once every 8 μs.

The microprocessor is a Motorola type M6800 (refer to M6800 product brochures for detailed information). The processor receives instructions and data from the ROM, writes data to and reads data from the RAM, and controls the other functional blocks. When power is applied to the DTO, R12, C25 holds $\overline{RESET}$ (K2-40) low to initialize the 6800. The timing generator provides DBE, and clocks Ø1 and Ø2 through inverting transistor drivers. The processor outputs ROM, RAM and I/O addresses through 16 address lines A0 and A15. The processor reads and writes instructions and data through data lines D0 through D7. Output VMA indicates valid information is on the address bus and R/W indicates whether the processor is reading or writing data through the data bus. The other processor inputs and outputs are not used. Circuits H6, H5, L5 and L6 buffer the processor from the address and data buses.

The eight ROMs A2 through A9 are connected directly to the address bus to select one of the 2048 words in each ROM. If the processor is reading a word from ROM (indicated by H3-8 high) one of the ROMs will be selected by C1 and it will output a word onto the data bus through B1.

Trace data, display data and numerous temporary variables are stored in the dynamic RAMs D4, E1, F1, H8, J1, K4, L7 and M2. These memories may be accessed twice during each processor cycle. During the first half cycle the RAMs are connected to the data bus for a DMA read (DMA is always a read) and during the second half for a processor read or write. Each RAM access requires the sequential application of the low and high order address bits through B2 and A10. The low order addresses are strobed by $\overline{RAS}$ and the high order by $\overline{CAS}$; if the processor requests a write, $\overline{WRITE}$ will be low during the second $\overline{RAS}$ - $\overline{CAS}$ cycle. Refer to the Timing Generator in Figure 4.7. Data from the RAMs drive the data bus through H7. The DMA channel provides the memory refresh.

Memory block decoder N5 divides the 65K word address space into eight segments shown in Table 4.5. N5 outputs are active only when VMA and $\overline{DMA}$ (L3-7) are true.

1. Front Panel Interface. $\overline{RP}$ (N7-6) selects reads of the front panel switches. WP (N7-4) selects writes to the front panel LEDs.

2. Input PCB Interface. $\overline{RI}$ (N8-6) selects reads of the Input PCB status and data. $\overline{WI}$ (N8-8) selects writes to the input PCB.

3. Tape Unit Interface. Refer to Appendix (X) for functions of specific Tape Unit signals.

See Table 4.6 for tape unit control signals.

4. $\overline{Read\ Bus\ Enable}$ T. (L1-6) enables the output of data from the Tape unit to the data bus (D0 through D7). L1-12 puts tape unit status information on the bus via M1.

5. DMA Counters. The display unit accesses RAM every 8 us through the DMA channel. The word to be accessed is determined by either one of two counters, 8-bit counter E5, E6 for control bytes and display characters or the 12-bit counter E8, E10, E9, for trace information. The 8-bit counter is reset at the start of each display cycle by $\overline{LAR1D}$ and

Table 4.5

Output	Address A15	A14	A13	VMA	$\overline{DMA}$	
0	0	0	0	1	1	RAM 0 to 8K
1	0	0	1	1	1	RAM 8K to 16K
2	0	1	0	1	1	Front Panel Switches and Lights
3	0	1	1	1	1	Input Board Control and Data
4	1	0	0	1	1	ROM 0 to 8K
5	1	0	1	1	1	ROM 8K to 16K
6	1	1	0	1	1	Tape Unit
7	1	1	1	1	1	ROM - Restart Vector for μP

Table 4.6 Tape Unit Control Signals

N1 Output	A2	A1	A0	Signal	Function
0	0	0	0	$\overline{LD\ W\ BUF\ T}$	Load Write Buffer
1	0	0	1	$\overline{RES\ T}$	Reset Tape Unit
2	0	1	0	$\overline{RUN\ T}$	Run Tape
3	0	1	1	$\overline{STOP\ T}$	Stop Tape
4	1	0	0	-	Set Read Latch
5	1	0	1	-	Reset Read Latch
6	1	1	0	-	Set Forward Latch
7	1	1	1	-	Reset Forward Latch

is incremented as required when ETAR1D and MP are high. The lower 8 bits of the 12-bit counter (E8, E10) are preset from the data bus by LAR2AD. The 12-bit counter increments as required when EPAR2D and ETAR2D are high. MD(J2-22) selects whether the 8 or 12 bit counter is connected to the address bus during a DMA cycle.

4.3.5 Power Supply

The Power Supply supplies seven voltages and two control signals to the DTO circuits. The seven voltages and current ratings are:

Voltage		Current
+5 V	± 0.25 V	at 8 A
-2 V	± 0.08 V	at 0.7 A
-5.2 V	± 0.2 V	at 2.3 A
+15 V	± 0.6 V	at 0.2 A
+15 V	(Tape)	at 1 A pulse
+12 V	± 0.5 V	at 0.4 A
-15 V	± 0.6 V	at 0.2 A

Refer to the schematic in Section VIII. Power to the DTO is supplied by conventional utility service and may be 100 to 240 V and 50 or 60 Hz. The input power module is used to connect the appropriate primary winding of T1 via an integral printed circuit board, protect the DTO from damage by a replaceable fuse, and reject power line noise with the integral filter. Proper fan voltage is also selected by the input module. The secondaries of T1 are rectified by CR1, 3, 4, 5, and 6 to provide the following approximate voltages:

Voltage	Filter Capicitor
+9 V	C1
-10 V	C2
+20 V	C3
-20 V	C9

The filter capacitors reduce the ripple to the regulators. Six regulators are used to produce the seven output voltages. All but the +5 V regulator are three-terminal integrated circuit devices that set the output voltage to the required value and limit their output current to prevent their destruction and protect the load.

The +5 V regulator conducts current to the load through Q1. The output voltage is compared to the -5.2 V output by resistors R6 and R11 and operational amplifier U1-1. If the output voltage is too low, U1-1 output goes positive increasing the current in Q2 and Q1 until the output is high enough. In the event that excessive current is required by the load, sufficient voltage is dropped across resistor R3 to cause U1-7 to go positive, forward biasing CR2. Current through CR2 increases the voltage at U1-2 so that U1-1 decreases the current in Q2 and Q1. The current limit is set to "fold back" so that less current is supplied into a short circuit than +5 V.

To prevent the DTO from being used with faulty power supplies, the circuitry associated with U2 holds the power on preset line ($\overline{POP}$) low whenever the +12 V, +5 V, -2 V, or -5.2 V supply is unusually low. Each voltage is compared to the voltage of the 5.1 V zener CR9. If one of the voltages is low the corresponding output of U2 will forward bias the diode (CR10, 11, 12 or 13) and turn on Q10.

It is possible for current to flow through the read/write head in the tape drive if the +5 V supply goes low before the +15 V to the tape unit. To prevent this, the +5 V supply is compared to the voltage of 5.1 V zener diode CR7. If the +5 V supply goes low, Q8 will turn on, which in turn turns on Q9. The collector of Q9 is connected into the Tape drive electronics to disable the write circuitry.

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